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Readout Electronics for Pixel Detectors in Deep Submicron and 3D Technologies

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***Abstract*—We have designed, fabricated in 90 nm technology and tested a prototype ASIC for readout of semiconductor pixel detectors for X-ray imaging applications. The 4mm x 4mm readout IC is working in single photon counting mode and contains a pixel matrix of 1280 readout channels with dimensions of 100 µm × 100 µm each. We present the architecture, the measurement results of this IC and our conclusions. To make this chip more attractive for novel experiments, we need to further increase single pixel functionality and at the same time reduce the pixel area. This leads us to the 3D technology with at least two layers: analogue and digital and additionally the sensor layer. We present the concept of the 3D hybrid pixel chip design with small pixel size and the ability to build a dead-space free large area pixel matrix.**

***Keywords*—Hybrid pixel detectors, deep submicron technology, 3D.**

I. Introduction

THE X-rays are widely used in many research fields like medicine, bioengineering, physics, material research etc. The continuously growing demand for new solutions in the mentioned fields requires new solutions for X-ray detection systems. Researchers around the world are trying to improve existing designs by making them more advanced, complex and reliable. As new solutions are taken into account, the semiconductor systems are popular because of the functionality which is placed in very small pixel area. We can distinguish one dimensional systems, where the sensor is covered by metal strips connected to readout electronics, and two dimensional ones where the detector is connected to the matrix of sensors. Hybrid pixel detectors working in single photon counting mode are very attractive for many applications. They usually contain a sensor connected to an ASIC made as a 2D array of pixel cells working as a multichannel readout electronics (Fig. 1). Such systems are commonly known and today many solutions are available. We have entered into the field of 2D X-ray detectors systems in 2008 and since then 2 prototype chips have been designed, fabricated in 90 nm technology and then tested. Our conclusions allow us to put few ideas about how to make the solution of readout electronics better. The first section contains description of latest prototype ASIC. The measurement results are shown in section II together with continuous mode of operation and data throughput consideration. The last section contains the description of possible solutions for making the system better and more attractive for novel research projects.

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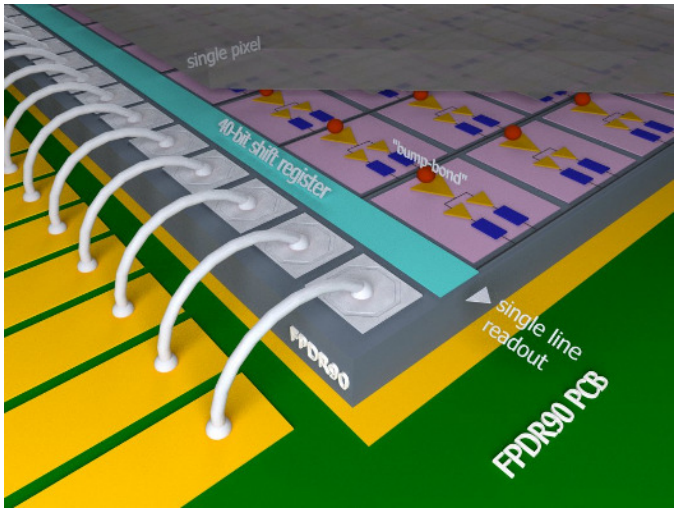


Fig. 1. The idea of hybrid pixel detector with FPDR90 chip.

II. Prototype IC Architecture

A. FPDR90 Description

We have designed two chips for 2D imaging applications [1], [2]. The first one is called PXD90, and the second one is called FPDR90 (Fast Pixel Detector Readout 90 nm). Those ASICs were designed with the functionality necessary to be attractive for readout electronics in hybrid detectors systems. This electronics can be characterized by a few critical parameters like: uniformity, noise, count rate, dead-time, power consumption, number of discriminators, position resolution. To make an attractive solution all mentioned parameters should not be worse when comparing to other existing solutions [3]–[5]. However, to make those parameters competitive, the functionality should be complex and therefore the single pixel size is growing. To overcome this limitation we decided to design our chips in the submicron technology and we have chosen the 90 nm CMOS process.

The FPDR90 is built as an array of 1280 silicon detector readout cells working in single photon counting mode. Keeping in mind critical parameters and reasonable functionality the single pixel area was chosen to be 100 µm x 100 µm. The single channel (see Fig. 2) consists of a fast charge sensitive amplifier (CSA) with modified Krummenacher feedback circuit [6], an AC coupling stage with gain control, a main

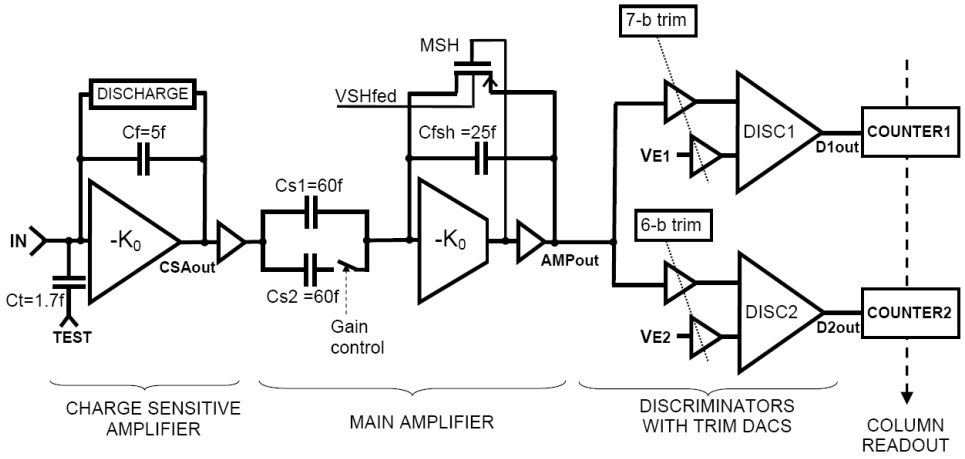


Fig. 2. Single channel architecture of FPDR90 chip.

amplifier, two independent discriminators with two correction DACs followed by two individual 16-bit counters.

The total chip area is 4 mm × 4 mm and it is divided for the pixel cells (32×40 pixels) and the control logic with main 40-bit shift register and the connection pads placed at the bottom of the chip.

B. FPDR90 Parameters Considerations

Our design works in single photon counting mode, where we decided to use two discriminators which indicate pulses higher than certain threshold. The common problems in such architecture are the noise and channel to channel uniformity which has its source in the nature of the fabrication process. In the design we decrease the channel to channel spread by applying AC coupling between the CSA and the main amplifier together with the offset correction circuits placed in each channel just before each discriminator. This solution allows one to obtain very good uniformity. Different effect occurs when the X-ray intensity is very high. Then, the mismatch of the CSA feedback discharge circuit causes different pulse width and therefore different channel performance. Keeping in mind the demand of high count rate, the discharge circuit was design as the Krummenacher feedback modified for the correction functionality to reduce the mismatch of the effective discharge time. The noise is minimized by the CSA optimization, where the main contribution is caused by the input transistor.

C. Detailed CSA Architecture

The charge sensitive amplifier uses a folded cascode configuration as a core – see Fig. 3. For the input transistor M1 we chose the transistor with the length of L = 200 nm (two times larger than the minimum) to reduce possible noise increase due to short channel effects and increase output resistance r_{ds1} of this transistor.

To minimize the noise contribution from M4 transistor it was pushed into linear region by making W/L = 1.44 µm/20 µm. This is unusual in such a design, but it allows reducing transconductance g_{m4} of M4 transistor (keeping at the same time relatively high its output resistance $r_{ds4} = 1/g_{ds4}$).

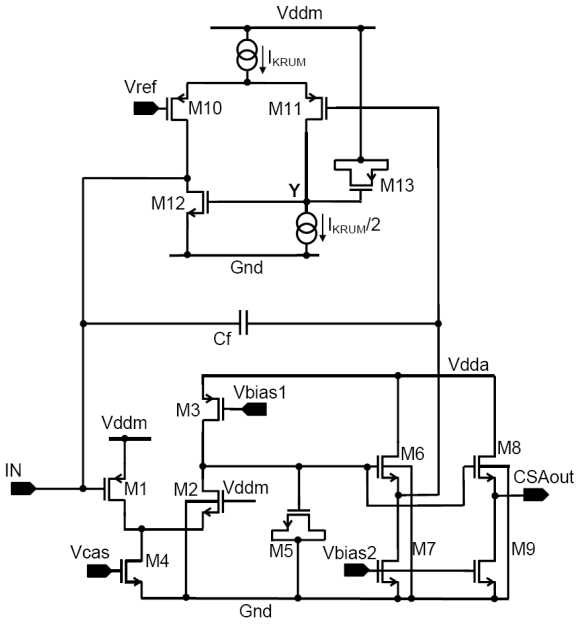


Fig. 3. CSA with the Krummenacher feedback.

For this design the folded cascode has the gain $|K_0| = 194\,V/V$ and with the dominant pole equals $f_0 = 2.92\,MHz$. These numbers give the gain-bandwidth of the folded cascode itself $GBW_{core} = |K_0| \times f_0$ equal to 0.57 GHz.

The left branch of the folded cascode operates with power supply voltage Vddm = 0.8 V to reduce the power consumption, while the right one works with Vdda = 1.2 V. The feedback loop of the CSA consists of the capacitor $C_f = 5fF$ and the Krummenacher feedback circuit. This structure has two feedback paths:

- resistive path of $R_f \approx 2/g_{m10}$ to discharge the C_f capacitor, where $g_{m10} = g_{m11}$ is transconductance of M10 (M11) transistor,
- inductive path for the detector leakage current compensation, so that DC detector leakage current flows into the

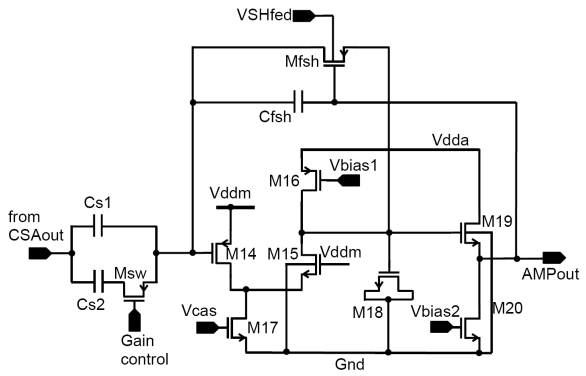


Fig. 4. Main amplifier scheme.

drain of M12 rather than into the R_f equivalent feedback resistance.

The equivalent scheme of the active feedback contains both the R_f equivalent feedback resistance and the L_f inductance of the value

$$L_f = \frac{2\,C_{g13}}{g_{m10}\,g_{m12}} \tag{1}$$

where C_{g13} = 2.8 pF is the gate capacitance of M13 and g_{m12} is the transconductance of M12. For the nominal settings of the current I_{krum} = 21 nA, the equivalent feedback resistance and inductance are $R_f \approx 6\,M\Omega$ and $L_f \approx 52H$ respectively.

D. Main Amplifier Architecture

The main amplifier is AC-coupled to the CSA stage to limit the DC offsets propagation – see Fig. 4. The series capacitors C_{s1} and C_{s2} are 60 fF each. The switch Msw allows to operate the circuit in low or high gain mode. The shaper core is based on the folded cascode with the transistor dimensions and the bias conditions as in the CSA stage. The feedback capacitor C_{fsh} is equal to 25 fF.

The novel approach is a resistive feedback based dynamic biasing. The effective resistance of Mfsh (W/L = 0.12 µm / 9.7 µm) is about $R_{fsh} \approx 25\,\mathrm{M\Omega}$. It can be controlled to some extent via the transistor bulk (VSHfed line). To keep this resistance constant even in the case of large positive pulses at the main amplifier output the signal is applied at the same time to the gate and the source of Msfh with some DC shift (gate-source voltage drop of M19 transistor $V_{gs19} \approx 290mV$).

At the output of main amplifier there is a simple correction circuit (see Fig. 5) which is based on two source followers with coupled control of their bias currents. The trim DAC current I_{trim} is subtracted from the first branch (source follower M21) and is added to the second one (source follower M22). As a result the DC differential voltage at the discriminator input is nearly linear function of the trim DAC correction current. It is important to keep a minimum value of the drain current in the source follower M21, because it drives the discriminator input. The maximum value of I_{trim} current is controlled by an external resistor.

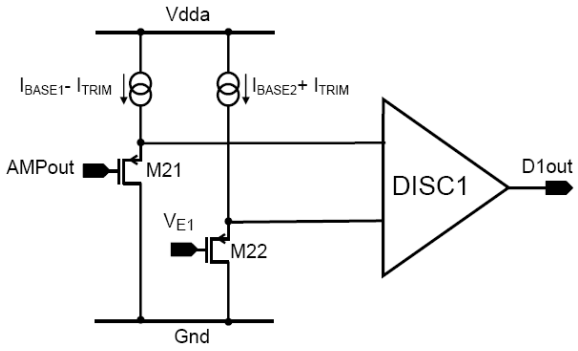


Fig. 5. Offset correction circuit at the discriminator input.

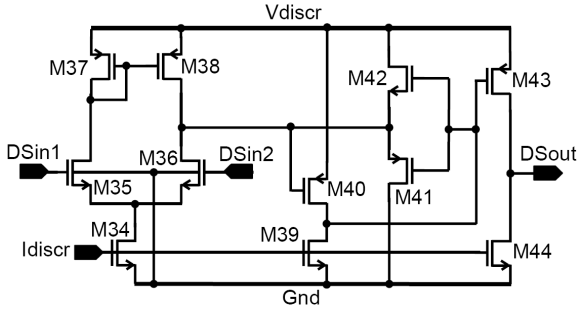


Fig. 6. Scheme of the discriminator.

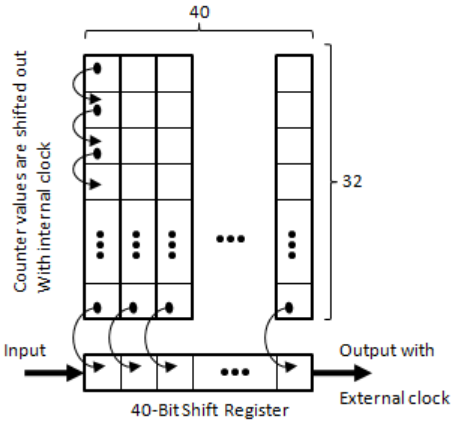


Fig. 7. The idea of FPDR90 data transmition.

E. Discriminator Scheme

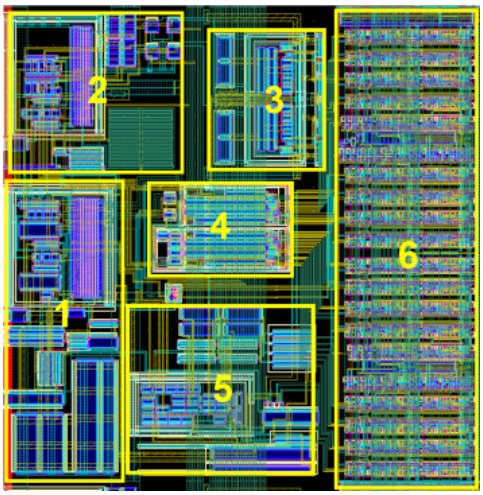
The discriminator (see Fig. 6) consists of three parts:

– input OTA to convert voltage signal to current signal (transistors M34-M38),
– current discriminator (transistors M39-M42),
– output amplifier (transistors M43 and M44) to drive properly a logic gate.

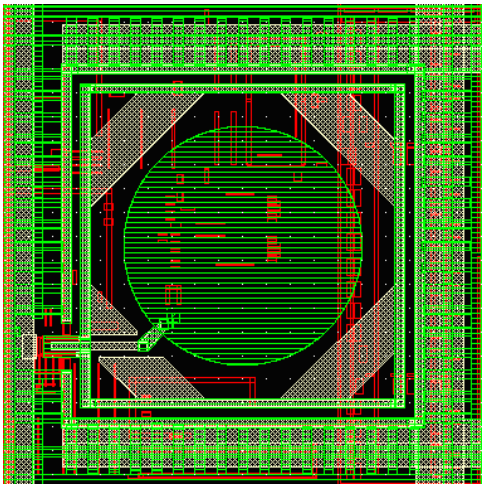
The maximum current in the last stage is limited to 0.7 µA to reduce the current spikes (on power supply lines) generated during comparator switching.

F. Data Readout

The FPDR90 is still only the prototype, so for testing and safety purposes we used many external bias lines which



(a)



(b)

Fig. 8. Layout of single pixel: (a) (MET4-MET9 are removed for better visibility): 1 – CSA, 2 – main amplifier, 3 – discriminators, 4 – trim DACs, 5 – reference blocks, 6 – counters, (b) (MET7-MET9) input stud bonding pad and metal shielding layers.

require pads for wire-bonding to a dedicated PCB. Because of those additional pads we used a single digital LVDS data output only, what of course limits the data throughput. The idea of data processing in the chip is shown in Fig. 7. The FPDR90 has 40 columns which consist of 32 pixels each. During the readout of the pixel matrix, with one cycle of the internal clock the data are transmitted from each pixel down to its neighbor, and from each column at the bottom to the 40-bit shift register. From this register the data are read out with an external clock, which has 40 times higher frequency than internal clock due to transmitting the 40-bit long word in one internal clock cycle.

III. Layout

The ASIC is designed in a 90 nm CMOS process. Its total area is 4 mm × 4 mm. Each pixel contains about 1800 transistors and measures 100 µm by 100 µm. The floor plan of a single pixel is shown in Fig. 8(a). The metal layers M4 to M9 are used for distribution of power supplies, shielding of the IC and stud bump bonding pad (see Fig. 8(b)).

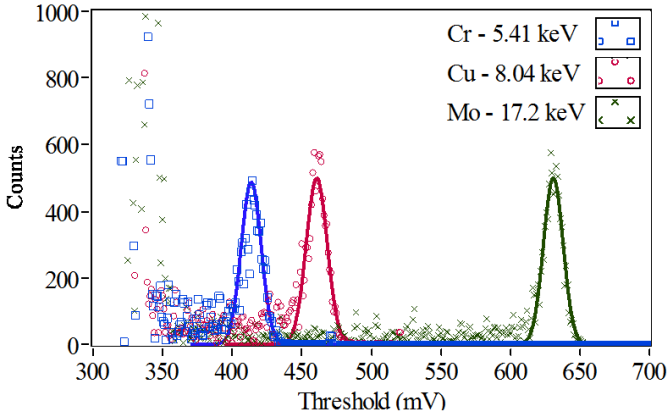


Fig. 9. Differential spectrum measured with FPDR90.

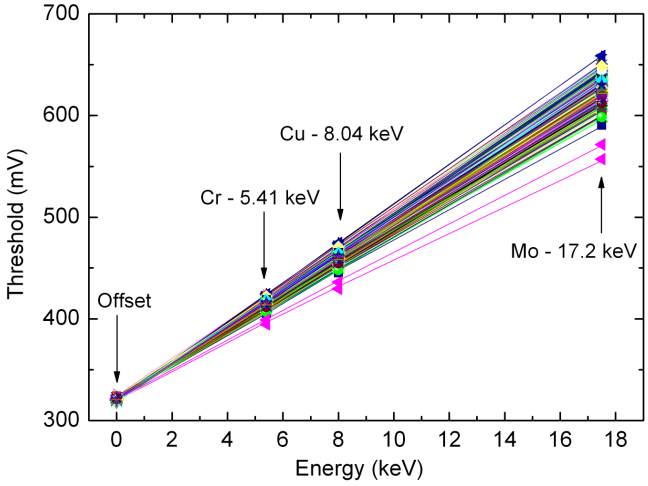


Fig. 10. Position of energy peaks for different pixels connected to the detector.

IV. Measurement

The circuit was tested and its functionality was proven. Example results – differential spectra measured with three different X-ray energies (namely Cr – 5.41 keV, Cu – 8.04 keV and Mo – 17.5 keV) are shown in Fig. 9.

A. Gain and Linearity of the FPDR90

For all pixels connected to the detector we have calculated the gain, the noise and their deviations. Example of the linearity of the gain is shown in Fig. 10. Here one can see also a very good uniformity of the DC level at discriminator input (offset – 0 keV value in Fig. 10). This is because the correction DACs values were calculated to eliminate the mismatch of the noise. Higher spread of 17.2 keV energy peaks is caused by the channel to channel gain spread. This is not a critical issue, because in practical applications both threshold are set close to each other, and therefore the correction for certain energy is needed.

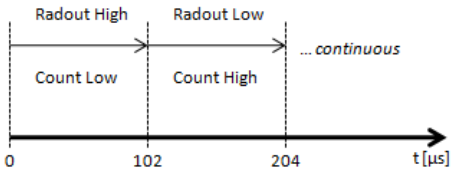


Fig. 11. Timing in continuous readout mode.

For nominal bias conditions the power consumption is 42 µW per pixel. The mean gain measured for the high and low gain setting is 64 and 32 µV/e$^-$ respectively. The measured mean ENC (equivalent noise charge) for all pixels connected to the detector is 106 e$^-$ rms and 107 e$^-$ rms in the high gain and low gain mode respectively. For the pixels not connected to the detector the ENC are 91 e$^-$ rms and 95 e$^-$ rms in the high gain and the low gain mode respectively.

B. Continuous Readout Mode

The architecture of the digital section of the FPDR90 allows one to readout the data continuously and provides a dead-time free acquisition. This was possible by making two independent counters groups (named Low and High) that can be individually configured either as shift registers, which allow to readout the data, or ripple counters, that count incoming pulses. The timing in the continuous mode of operation is presented in Fig. 11. One of the counters, here counters Low, is set as the ripple counter and the second as a shift register. During this time counter Low increments its value with discriminator pulses, and counter High shifts the data out of the chip. After reading all the counterâ€™s High bits, the operation of both counters is switched. This situation can be repeated continuously. During the tests we did not observe any problems with crosstalk from digital to analog blocks.

The communication with our IC is tested with the clock frequency up to 200 MHz and due to digital data generator limitation we could not go any faster . However in the continuous mode the frame rate is 9 kHz (reading 16-bits data from each pixel) and 72 kHz . (reading only 1-bit data from each pixel). In the FPDR90 only one output line is used, what limits the data throughput from the chip to 200 Mbps. This number can be multiplied in the future designs by the number of output lines e.g. for 8 output lines the data throughput would be 1.6 Gbps.

C. FPDR90 Summary

FPDR90 chip parameters and performance are summarized in the Table I. Low peaking time, low noise, high gain and good uniformity makes this chip one of the best reported in the literature.

TABLE I
SUMMARY OF THE FPDR90 PARAMETERS

Technology	CMOS 90 nm
Die size	4 mm × 4 mm
Total number of transistors	> 2 million
Pixel Unit Cell (PUC) dimientions	100 µm × 100 µm
Number of PUCs	1280
Supply voltage: core / IO	0.8 & 1.2 / 2.5 V
Power dissipation per PUC	42 µW
Peaking time	28 ns
Equivalent Noise Charge: (high / low gain)	
– without detector	91 / 95 e$^-$ rms
– with stud bump bonded detector	106 / 107 e$^-$ rms
Gain in high / low gain mode	64 / 32 µV/e$^-$
Offset spread (after correction)	
– with 7-bit trim DAC	0.76 mV rms
– with 6-bit trim DAC	1.16 mV rms
Front-end dead time (paralyzable model)	
– standard setting (I_{krum} = 21 nA)	342 ns
– fast setting (I_{krum} = 162 nA)	117 ns
Number of discriminators per channel	2
Counter capacity	2 × 16 bit
Readout dead time	
– standard mode (single output)	218 µs
– continuous mode	0
Communication	LVDS standard with 200 MHz clock

V. CONSIDERATION OF THE DESIGN OF AN ASIC IN 3D TECHNOLOGY

The design presented in previous sections contains the functionality necessary for many different applications in physics and other research fields. However, permanently growing demands for the solution of smaller pixel size and bigger detector area require continuous modifications of designs. To make our solution even more attractive for novel experiments few changes are necessary: increase of the position resolution by decreasing single pixel size and adding more functionality in the digital part to make possible building large area detectors with minimum number of bad pixels.

A. Smaller Pixel Size

Presented solution has certain functionality which is expected from a single photon counting mode readout ASIC, and it not advisable to reduce it. There are two possible ways for making single pixel cell smaller maintaining the same functionality: using smaller technology node or using a 3D technology. The FPDR90 is made in 90 nm CMOS process and from designers point of view there would be no visible profit in the analog part by going into smaller transistor size. There are few reasons:

- matching – better results can be achieved with larger transistors. Going into smaller technology features does not improve matching,
- newer technologies use lower power supply voltage what leaves smaller range for the signal processing, and are more demanding from analog point of view,
- new technologies below 90 nm are extremely expensive for prototyping.

Those issues can be problematic for ASICs designers and even though it could be very interesting to challenge them, today the price is still beyond capabilities of many researchers and

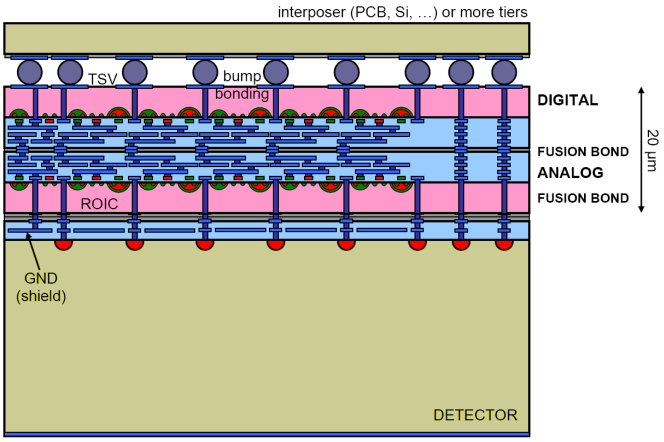


Fig. 12. Cross-section of a 4-side buttable pixel detector tile.

even if the design would be successful, the space saved would not be significant.

Second possibility of making the single pixel smaller is to divide its functionality among two or more silicon layers and then integrate them in 3D process which is based on through silicon vias (TSV). An example of such a solution is shown in Fig. 12, which shows a schematic cross section of 4-side buttable pixel detector tile proposed in VIPIC IC project [7], [8]. This possibility is available for quite some time now and as concluded in [7] it may be the best method for boosting performance of ICs.

B. Functionality Increase

In the design of a pixel detector readout ASIC in 3D technology the size of single pixel cell could be decreased twice – from 100 µm × 100 µm to 75 µm × 75 µm . The reason is, that the analog blocks, which now consume approximately 66% of the pixel area could be reduced when separated from digital block by the space used e.g. to decouple digital noise.

Assuming, that the vertically integrated circuit could have the pixel size 75 µm × 75 µm , the functionality of the digital part, which now consumes about 33% of the pixel area, could be increased. In the digital blocks a few changes are expected:

- supplying the readout with single pixel biasing. Now all the data read from single column is daisy-chained through pixels, what can cause the whole column corruption when single pixel is broken. If it would be possible to bypass the data, the yield would increase,
- redundancy in critical points in the data readout. In current design the data from columns are written bit by bit to one shift register which is placed at the bottom of the chip and then the data is readout from this shift register with much higher speed (Fig. 7). It is important, to find critical points in the data transmission which can cause entire column collapse when broken. Those points need to be redundant,
- increase the readout speed by applying the double data rate or/and higher external frequency. This functionality seems to be possible and since we do not see the limit of 200 MHz in current design the expected readout speed could be increased up to 500 MHz,
- Remove the connection pads from the bottom of the chip and placing them at the back side of the chip. This enhancement is possible with the use of TSVs and it gives us two very important improvements: removes not active area of the chip what make possible to build large area detectors with no dead inter chip space, and makes possible to significantly increase the readout speed by radically increasing number of outputs, e.g. if we increase the number of outputs in our current design up to 20 we increase the data throughput up to 4 Gbps.

VI. Conclusion

We presented our achievement in the designing of the pixel readouts working in single photon counting mode. The limits which we have reached do not allow to decrease the single pixel size or to increase its functionality. This pushes us to the vertically integrated ICs what seems to be a solution for continuously growing demands of very small pixel size and high functionality. Additionally, the 3D process allows eliminating the space necessary for connecting the chip to external singles by placing the connection pads at the back side of the chip and then bump-bonding to dedicated PCB. This solution makes building a dead-space free large area hybrid detector possible.

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