POLISH ACADEMY OF SCIENCE
COMMITTEE FOR ELECTRONICS AND TELECOMMUNICATIONS

ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY

KWARTALNIK ELEKTRONIKI I TELEKOMUNIKACJI

VOLUME 53 — No 4

WARSAW 2007

Address of Editorial Office
00-665 Warszawa, ul. Nowowiejska 15/19 Politechnika, pok. 470
Instytut Telekomunikacji, Gmach im. prof. JANUSZA GROSZKOWSKIEGO

Editor-on-duty
Wednesdays and Fridays
From 2pm to 4pm
Phone number: (022) 234 77 37

Telephone numbers
Editor-in-Chief: 0607240533
Deputy Editor-in-Chief: 0502660096
Responsible Secretary: 0500044131

Ark. wyd. 6,25 Ark. druk. 5,00	Podpisano do druku w grudniu 2007 r.
Papier offset. kl. III 80 g. B-1	Druk ukończono w grudniu 2007 r.

Publishing
Warszawska Drukarnia Naukowa PAN
00-656 Warszawa, ul. Śniadeckich 8
Tel./fax: 628-87-77

KO — czł.
r hab. inż.
D SĘDEK,
PAN, prof.

IMPORTANT MESSAGE FOR THE AUTHORS

The Editorial Board during their meeting on the 18th of January 2006 authorized the Editorial Office to introduce the following changes:

1. PUBLISHING THE ARTICLES IN ENGLISH LANGUAGE ONLY

Starting from No 1'2007 of E&T Quarterly, all the articles will be published in English only.

Each article prepared in English must be supplemented with a thorough summary in Polish (e.g. 2 pages), including the essential formulas, tables, diagrams etc. The Polish summary must be written on a separate page. The articles will be reviewed and their English correctness will be verified.

2. COVERING THE PUBLISHING EXPENSES BY AUTHORS

Starting from No'2007 of E&T Quarterly, a principle of publishing articles against payment is introduced, assuming non-profit making editorial office. According to the principle the authors or institutions employing them, will have to cover the expenses in amount of 760 PLN for each publishing sheet. The above amount will be used to supplement the limited financial means received from PAS for publishing; particularly to increase the capacity of next E&T Quaterly volumes and verify the English correctness of articles. It is neccessary to increase the capacity of E&T Quarterly volumes due to growing number of received articles, which delays their publishing.

In case of authors written request to accelerate the publishing of an article, the fee will amount to 1500 PLN for each publishing sheet.

In justifiable cases presented in writing, the editorial staff may decide to relieve authors from basic payment, either partially or fully. The payment must be made by bank transfer into account of Warsaw Science Publishers The account number: Bank Zachodni WBK S.A. Warszawa Nr 94 1090 1883 0000 0001 0588 2816 with additional note: "For Electronics and Telecommunications Quarterly".

Editors

Elec
Elektrot
The
of Polish
Quarterl
theoretic
recognis
tronics,
The
young re
The
critical e
branch
mathema
and ISO
All
specialis
The pub
Science
The
telecomm
Moreove
Each
distributi
author. T
accessibl
The a
and the
publicati
editorial
The a
office ad

Dear Authors,

Electronics and Telecommunications Quarterly continues tradition of the "Rozprawy Elektrotechniczne" quarterly established 53 years ago.

The E&T Quarterly is a periodical of Electronics and Telecommunications Committee of Polish Academy of Science. It is published by Warsaw Science Publishers of PAS. The Quarterly is a scientific periodical where articles presenting the results of original, theoretical, experimental and reviewed works are published. They consider widely recognised aspects of modern electronics, telecommunications, microelectronics, optoelectronics, radioelectronics and medical electronics.

The authors are outstanding scientists, well-known experienced specialists as well as young researchers – mainly candidates for a doctor's degree.

The articles present original approaches to problems, interesting research results, critical estimation of theories and methods, discuss current state or progress in a given branch of technology and describe development prospects. The manner of writing mathematical parts of articles complies with IEC (International Electronics Commision) and ISO (International Organization of Standardization) standards.

All the articles published in E&T Quarterly are reviewed by known, domestic specialists which ensures that the publications are recognized as author's scientific output. The publishing of research work results completed within the framework of *Ministry of Science and Higher Education* GRANTs meets one of the requirements for those works.

The periodical is distributed among all those who deal with electronics and telecommunications in national scientific centres, as well as in numeral foreign institutions. Moreover it is subscribed by many specialists and libraries.

Each author is entitled to free of charge 20 copies of article, which allows for easier distribution to persons and institutions domestic and abroad, individually chosen by the author. The fact that the articles are published in English makes the quarterly even more accessible.

The articles received are published within half a year if the cooperation between author and the editorial staff is efficient. Instructions for authors concerning the form of publications are included in every volume of the quarterly; they may also be obtained in editorial office.

The articles may be submitted to the editorial office personally or by post; the editorial office address is shown on editorial page in each volume.

Editors

CONTENTS

Poi

tio
str
pro
Th
lin
cal
up
wit
the

Ke

For
network
system s
Bandwic
defined
define c
equivale
[2, 3, 7]

ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY, 2007, 53, no 4, pp. 339–360

Point-to-Point and Point-to-Group Blocking Probability in Multi-service Switching Networks with BPP Traffic

MARIUSZ GŁĄBOWSKI

Chair of Communications and Computer Networks
Poznań University of Technology
ul. Polanka 3, 60-965 Poznań, Poland
mariusz.glabowski@et.put.poznan.pl

Received 2007.08.13
Authorized 2007.11.14

This paper presents three approximate calculation methods of occupancy distribution and blocking probability in switching networks which are offered multi-service traffic streams generated by Binomial (Engset) & Poisson (Erlang) & Pascal traffic sources. The proposed methods belong to the class of methods known as the effective availability methods. The basis of the proposed calculation algorithms is the occupancy distribution in interstage links as well as in the outgoing links (forming outgoing directions). These distributions are calculated with the help of the full-availability group model and the limited-availability group model. The results of analytical calculations of the blocking probabilities are compared with the simulation results of three-stage switching networks, and, therefore, the validity of the assumptions used in the model is proved.

Keywords: BPP traffic, switching networks, blocking probability

1. INTRODUCTION

For the analytical modelling of traffic characteristics of multi-service switching networks the multi-rate models [1, 2, 3, 4, 5, 6] are mainly used. In these models the system services call demands having an integer number of the so-called BBUs (Basic Bandwidth Units). In accordance with the bandwidth discretisation [2], the BBU is defined as the greatest common divisor of all call demands offered to the system. To define call demands of sources with variable bit rates, it is proposed to determine an equivalent bandwidth for particular classes of traffic streams generated by the sources [2, 3, 7].

Multi-service switching networks were the subject of many analyses [8, 9, 10, 11, 12, 13, 14]. The analytical methods of determination of traffic characteristics of such systems can be classified into two groups. In the first one time-effective algorithms of solving statistical equilibrium equations in a multi-dimensional Markov process are searched for. However, in spite of its great accuracy, this method cannot be used for calculations of larger systems which have practical meaning. The reason for this is an excessive number of states[1] in which a multi-dimensional Markov process occurring within the system can take place [8]. Methods of the other group consist in approximating a multi-dimensional service process by the appropriately constructed one-dimensional Markov chain, which is characterised by a product form solution [15, 16, 17]. Within the latter group, the most effective methods of switching networks calculations are the well-proven methods of the so-called effective availability [18, 19, 10]. The effective availability is defined as the availability in a multi-stage switching network in which the blocking probability is equal to the blocking probability of a single-stage network (grading) with the same capacity of the outgoing group and at analogous parameters of the traffic stream offered. The modern methods of calculating the effective availability are based on works [18], [19] and [20], where all the components of this parameter have been defined. In [10], the universal formulae for calculating the effective availability have been derived for arbitrary multi-stage switching networks carrying a mixture of different multi-rate traffic streams. On the basis of such formulae, the methods for multiservice switching networks with point-to-point, point-to-group and point-to-group with several attempts of setting up a connection have been proposed [10, 11, 12, 13, 14].

Despite numerous studies in analytical modelling of switching networks with multi-rate traffic, in most of the published papers known to the author, only the switching networks with an infinite source population have been analysed. However, in modern networks, the ratio of source population and the capacity of a system is often limited and the value of traffic load offered by calls of particular classes is dependent on the number of occupied bandwidth units in the group, i.e. on the number of in-service traffic sources. Such systems are described by the generalized Multiclass Engset Model (GMEnM) [21, 22, 23, 24, 25, 26]. One of the most exemplifying up-to-date systems of this kind is the Universal Mobile Telecommunications System (UMTS) – system in which obtaining of predefined Quality of Service parameters for particular services is accompanied with a necessity to limit the number of concurrent users serviced by a given base station. Simultaneously, the switching techniques used in the UMTS system (and in Asynchronous Transfer Mode in particular) allow to determine equivalent bandwidths for particular classes of call streams and, in consequence, to apply multi-rate models. The first method of point-to-group blocking probability calculation in switching networks with a finite source population, limited to the case of Engset

[1] A state of a system in the multi-dimensional state space is explicitly described by the number of calls of particular classes carried by the system.

traffic streams, was published in [27]. The analytical method of blocking probability calculation in switching networks with point-to-point selection and BPP traffic was proposed in [28].

In this paper, based on considerations presented in [27] and [28], the new methods of blocking probability calculation in the switching networks which are offered multi-rate traffic streams generated by a finite and an infinite population of traffic sources have been presented, i.e. PGBMF (Point-to-Group Blocking for Multi-rate traffic with Finite source population) method, PPBMF (Point-to-Point Blocking for Multi-rate traffic with Finite source population) method and PPFD (Point-to-Point blocking for multi-rate traffic with Finite source population – Direct method) method.

The proposed methods lead to the following general calculation algorithm in switching networks. Firstly, the effective availability is calculated for all traffic classes. Then the internal blocking probabilities for particular traffic streams are determined using simple combinatorial formulae (different in each of the proposed methods) which include the effective availability parameter. The external blocking for particular traffic classes are calculated using the occupancy distribution in outgoing directions which are modelled by the limited availability group. The presented algorithm of calculations immediately imposes further organization of the article. Section 2 presents models of link group in switching networks servicing multi-rate BPP (Binomial-Poisson-Pascal) traffic. In Section 3, the PGBMF, PPBMF and PPFD methods of blocking probability calculation in multi-service switching network with a finite and an infinite source population are proposed. In Section 4, the calculation results are compared with the simulation results of switching networks. Section 5 concludes the paper.

2. LINKS MODELS IN MULTISERVICE SWITCHING NETWORKS

2.1. LIMITED-AVAILABILITY GROUP WITH INFINITE POPULATION OF TRAFFIC SOURCES

Let us consider the limited-availability group (LAG) model, i.e. the system composed of k separated transmission links (Fig. 1). The system services call demands having an integer number of BBUs. Additionally, each of the links of the group has the capacity equal to f BBUs. Thus, the total capacity of the system is equal to $V = kf$. The system services a call – only when this call can be entirely carried by the resources of an arbitrary single link. The group is offered M independent classes of Poisson traffic streams having the intensities: $\lambda_1, \lambda_2, \ldots, \lambda_M$. The holding time for calls of particular classes has an exponential distribution with the parameters: $\mu_1, \mu_2, \ldots, \mu_M$. Thus, the mean traffic offered to the system by the class i traffic stream is equal to:

$$A_i = \lambda_i/\mu_i. \tag{1}$$

A class i call requires t_i BBUs to set up a connection.

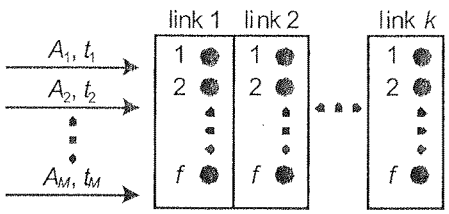

Fig. 1. A limited-availability group

The occupancy distribution in the considered system can be determined on the basis of the generalized Kaufman-Roberts recursion (GKRR) [16, 17]. The generalization consists in the introduction of relevant conditional (state dependent) state-passage probabilities $\sigma_i(n)$ between the adjacent states of the system into the Kaufman-Roberts recursion [16, 17]:

$$n[P_n]_V = \sum_{i=1}^{M} A_i t_i \sigma_i(n - t_i)\,[P_{n-t_i}]_V, \tag{2}$$

where $[P_n]_V$ is the probability of an event in which there are n busy BBUs in the system and $\sigma_i(n)$, the so-called conditional state-passage probabilities, is the probability of admission of class i call to the service when the system is found in the state n.

2.2. CONDITIONAL STATE-PASSAGE PROBABILITY

The conditional state-passage probability, that takes into account the dependence between call streams and the state of the system, determines part of the incoming call stream λ_i to be transferred between the states n and $n + t_i$ due to the specific structure of the limited-availability group. The parameter $\sigma_i(n)$ can be calculated as follows [10]:

$$\sigma_i(n) = 1 - (F(V - n, k, t_i - 1, 0)/F(V - n, k, f, 0)), \tag{3}$$

where $F(x, k, f, t)$ is the number of arrangements of x free BBUs in k links, calculated with the assumption that the capacity of each link is equal to f BBUs and each link has at least t free BBUs:

$$F(x, k, f, t) = \sum_{i=0}^{\left\lfloor \frac{x-kt}{f-t+1} \right\rfloor} (-1)^i \binom{k}{i} \binom{x - k(t-1) - 1 - i(f-t+1)}{k-1}. \tag{4}$$

Having the probabilities $\sigma_i(n)$, we can calculate the distribution $[P_n]_V$ and subsequently the blocking probability e_i for class i calls. The blocking state in LAG takes place when no link has sufficient number of free BBUs to service class i calls. Thus a state in which each link contains $(t_i - 1)$ free BBUs is already the blocking one. All the blocking states can be determined by the following condition:

$$V - k(t_i - 1) \leqslant n \leqslant V \tag{5}$$

and finally the blocking probability e_i for a class i stream can be calculated as follows:

$$e_i = \sum_{n=V-k(t_i-1)}^{V} [P_n]_V [1 - \sigma_i(n)]. \tag{6}$$

The diagram presented in Fig. 2 is appropriate to the GKRR (2) for the system with two call streams ($M = 2, t_1 = 1, t_2 = 2$). The $y_i(n)$ symbol denotes reverse transition rates of a class i service stream outgoing from state n. These transition rates for a class i stream are equal to the average number of class i calls serviced in state n. From Eq. (2) it results that the knowledge of the parameter $y_i(n)$ is not required for the determination of the occupancy distribution in LAG with multi-rate traffic generated by an infinite population of traffic sources. However, the value of this parameter, in a given state of the group, is the basis of the method applied in this paper for the occupancy distribution calculation in the group with a finite population of traffic sources. The parameter $y_i(n)$ can be determined on the basis of the statistical equilibrium equations in the considered group [29]:

$$y_i(n + t_i) = \begin{cases} A_i \sigma_i(n) [P_n]_V / [P_{n+t_i}]_V & \text{for} \quad n + t_i \leqslant V \\ 0 & \text{for} \quad n + t_i > V \end{cases} \tag{7}$$

Formula (7) determines the average number of class i calls serviced in the state $n + t_i$.

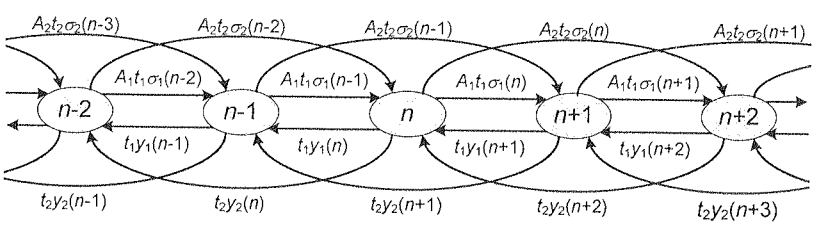

Fig. 2. A fragment of a diagram of the one-dimensional Markov chain in a multi-rate system ($M = 2, t_1 = 1, t_2 = 2$)

2.3. LIMITED-AVAILABILITY GROUP WITH BPP TRAFFIC

This section proposes an approximate recursive algorithm that allows to determine the occupancy distribution in the limited-availability group which is offered several classes of Erlang, Engset and Pascal traffic (BPP traffic) with different number of demanded BBUs to set up a connection. We start the present considerations with a short presentation of basic assumptions for the multi-rate Engset and Pascal model.

2.3.1. Assumptions of Engset multi-rate model

Let us consider now the system servicing multi-rate traffic generated by a finite population of sources. Let us denote as N_j the number of sources of class j, the calls of which require t_j BBUs for service. The input traffic stream of class j is built by the superposition of N_j two-state traffic sources which can alternate between the active (busy) state ON (the source requires t_j BBUs) and the inactive state OFF (the source is idle). When a source is busy, its call intensity is zero. Thus the arrival process is state-dependent. The class j traffic offered by an idle source is equal to $\alpha_j = \Lambda_j/\mu_j$, where Λ_j is the mean arrival rate generated by an idle source of class j and $1/\mu_j$ is the mean holding (service) time of class j calls. In the considered model, the holding time for calls of particular classes has an exponential distribution. Thus, the mean traffic offered to the system in the state of n BBUs being busy by idle class j traffic sources is equal to:

$$A_j(n) = (N_j - n_j(n))\alpha_j, \tag{8}$$

where $n_j(n)$ is the number of in-service sources of class j in state n.

2.3.2. Assumptions of Pascal multi-rate model

Considering Pascal traffic streams we also assume a finite number of traffic sources. As in the Engset case, we assume that at the very beginning there are S_q sources of class q requiring t_q BBUs. Each idle source generates calls with intensity γ_q. The holding time has an exponential distribution with the intensity μ_q. Contrary to Engset Multi-rate Model, in the Pascal case, arrival intensity of particular traffic classes increases with the occupancy state of the system. This means that the arrival intensity of a class q is equal $(S_q + n_q(n))\gamma_q$, where $n_q(n)$ is the number of in-service sources of class q in state n. Thus, the mean traffic offered to the system in the state of n BBUs being busy by class q traffic sources is equal to:

$$A_q(n) = (S_q + n_q(n))\beta_q, \tag{9}$$

where $\beta_q = \gamma_q/\mu_q$ is the mean traffic offered by an idle source of class q.

2.3.3. Assumptions of Erlang-Engset-Pascal multi-rate model

Let us consider the group with the capacity equal to V BBUs which is offered three types of traffic streams: M_1 Erlang (Poisson) traffic streams, M_2 Engset (Binomial) traffic streams and M_3 Pascal traffic streams. The mean arrival rate of class i Erlang traffic stream does not depend on the state of the system and is equal to λ_i, while the mean arrival rate $\lambda_j(n)$ of class j Engset traffic stream and the mean arrival rate $\lambda_q(n)$

of class q Pascal traffic stream depend on the number of calls being serviced in the following way:

$$\lambda_j(n) = (N_j - n_j(n))\gamma_j, \tag{10}$$

$$\lambda_q(n) = (S_q + n_q(n))\gamma_q. \tag{11}$$

In the model considered we assume that the holding time for calls of particular BPP traffic classes have an exponential distribution. The model of the system with multi-rate BPP traffic will be, in the further part of the paper, designated by symbol ErEnPaMLM.

2.3.4. Concept of determination of multi-service Erlang-Engset-Pascal distribution

As we can notice in Sections 2.3.1, 2.3.2 and 2.3.3, the dependence of the value of the offered traffic on the number of active sources in Engset and Pascal streams makes it impossible to apply directly the generalized Kaufman-Roberts formula. In this section we will discuss the idea of modelling multi-service switching networks by the application of the modified Kaufman-Roberts formula. The basis of this method is formed by a determination of an approximate method of determining the number of active traffic sources of a given class in Engset and Pascal streams.

Initially, we assume in the algorithm that the number of BBUs occupied in each of the states n by respectively calls of class j Engset stream and class q Pascal stream, is the same as the number of BBUs occupied by the equivalent Erlang stream generating the offered traffic with the intensity:

$$A_j = N_j\alpha_j, \tag{12}$$

$$A_q = S_q\beta_q, \tag{13}$$

which is equal in value to the traffic offered by all idle sources of class j Engset stream and class q Pascal stream.

The above adopted assumption also implies that the number of in-service $n_j(n)$ and $n_q(n)$ sources of class j and q, respectively, in the state of n BBUs being busy, can be approximated by the reverse transition rates $y_j(n)$ and $y_q(n)$, determined on the basis of Equation (7) for the equivalent Erlang streams (Equations (12) and (13)):

$$n_j(n) \approx y_j(n), \tag{14}$$

$$n_q(n) \approx y_q(n). \tag{15}$$

The determined values of $y_j(n)$ and $y_q(n)$ enable us to make the mean value of offered traffic dependent on the occupancy state of the group in the following manner:

$$A_j(n) = [N_j - y_j(n)]\alpha_j, \tag{16}$$

$$A_q(n) = [S_q + y_q(n)]\beta_q. \tag{17}$$

Having the traffic values $A_j(n)$ (Equation (16)) and $A_q(n)$ (Equation (17)), Equation (2) can be rewritten in the form that includes the traffic characteristics of Engset and Pascal traffic, namely:

$$n[P_n]_V = \sum_{i=1}^{M_1} A_i t_i \sigma_i(n - t_i)[P_{n-t_i}]_V + \sum_{j=1}^{M_2} A_j(n - t_j) t_j \sigma_j(n - t_j)\left[P_{n-t_j}\right]_V + \\ + \sum_{q=1}^{M_3} A_q(n - t_q) t_q \sigma_q(n - t_q)\left[P_{n-t_q}\right]_V . \tag{18}$$

The universal nature of Equation (18) should be particularly stressed. Depending on type of the offered traffic, the equation can determine the occupancy distribution in systems with just one type of traffic, for example only Pascal traffic, where $M_1 = 0$, $M_2 = 0$ and $M_3 \neq 0$), or in systems with the mixture of traffic from different types of sources as in, for instance, Engset and Pascal types of traffic, when $M_1 = 0$, $M_2 \neq 0$ and $M_3 \neq 0$).

2.4. FULL-AVAILABILITY GROUP

The full-availability group (FAG) is a discrete model of a single link that uses complete sharing policy [2]. This system is an example of a state-independent system in which the probability of admission of a new call does not depend on the number of busy bandwidth units in the system (as long as the system have enough BBUs to service a call of a given class). Therefore, the conditional state-passage probability $\sigma_i(n)$ in FAG is equal to 1 for all states and for each traffic class. Consequently, the occupancy distribution and blocking probabilities in FAG with an infinite and a finite source population can be calculated by the equations (18) and (6), taking into consideration the fact that: $\forall_i \forall_n \sigma_i(n) = 1$.

2.5. DISTRIBUTION OF AVAILABLE LINKS

On the basis of the occupancy distribution in LAG (18), the so-called distribution of available links is determined [10]. This distribution determines the probability $P(i, s)$ of an event in which each of arbitrarily chosen s links can carry the class i call. In order to calculate $P(i, s)$ distribution, it is indispensable to know the so-called conditional distribution of available links $P(i, s \mid x)$. This distribution determines the probability of

an arrangement of $x(x = V - n)$ free BBUs, in which each of s arbitrarily chosen links has at least t_i free BBUs, while in each of the remaining $(k - s)$ links the number of free BBUs is lower than t_i (Eq. (4)). Following the combinatorial consideration [10]:

$$P(i, s|x) = \frac{\binom{k}{s} \sum_{w=st_i}^{\Psi} F(w, s, f, t_i) F(x - w, k - s, t_i - 1, 0)}{F(k, x, f, 0)}, \tag{19}$$

where: $\Psi = sf, \text{if} x \geqslant sf, \Psi = x, \text{if} x < sf$.

On the basis of the distribution $P(i, s \mid x)$ and of the theorem of total probability, the distribution of available links $P(i, s)$ is equal to:

$$P(i, s) = \sum_{n=0}^{V} [P_n]_V P(i, s|V - n), \tag{20}$$

where $[P_n]_V$ is the occupancy distribution in the limited-availability group with BPP traffic streams.

3. SWITCHING NETWORK CALCULATIONS

In this section three approximate methods of blocking probability calculation in multi-stage switching networks with multi-rate BPP traffic are presented, i.e. PGBMF (Point-to-Group Blocking for Multi-rate traffic with Finite source population) method, PPBMF (Point-to-Point Blocking for Multi-rate traffic with Finite source population) method and PPFD (Point-to-Point blocking for multi-rate traffic with Finite source population – Direct method) method. The presented considerations are based on PGBMT, PPBMT and PPD methods, worked out in [10] and [12] for multiservice switching networks with traffic streams generated by an infinite source population.

The presented general outlines of calculations of switching networks consist in the reduction of calculations of internal blocking probability in a multi-stage switching network to the calculation of the probability in an equivalent switching network model servicing single channel traffic. Such an approach allows us to analyse multi-stage switching networks with multi-rate traffic with the use of the effective availability method.

3.1. BASIC ASSUMPTIONS

Let us consider a switching network with multi-rate BPP traffic (Fig. 3), consisting of the switches of $k \times k$ links. Let us assume that each of the inter-stage links has the capacity equal to f BBUs and that outgoing transmission links create link groups called directions. In the paper we have assumed that an interstage link can be modelled by the full-availability group and a direction can be modelled by the limited-availability group.

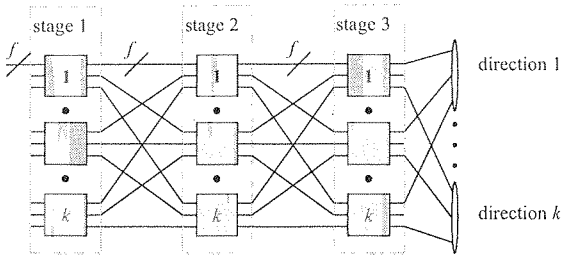

Fig. 3. A three-stage switching network

In general, switching networks can operate with a point-to-group or point-to-point selection. Let us consider first the switching network with a point-to-group selection. Following the control algorithm of this kind of selection [10], the control device of the switching network determines the first stage switch, on the incoming link of which a class i call appears (switch α). Then, the control system finds the last-stage switch (switch β) having a free outgoing link (i.e. the link comprising of at least t_i free BBUs) in a required direction. Next, the control device tries to find a connection path between switches α and β. If such a path does not exist, the control system begins the second attempt to set up a connection, i.e. the control system determines another switch β and tries to find a new connection path between switches α and β. The number of attempts is limited to the number of the last-stage switches having at least t_i idle BBUs in the considered direction. If such switches do not exist, a class i call is lost. In the case of a switching network with point-to-point selection, the number of attempts of setting up a new connection is limited to one.

3.2. POINT-TO-GROUP BLOCKING FOR MULTI-RATE BPP TRAFFIC – PGBMF METHOD

Let us consider a switching network with point-to-group selection and multi-rate traffic, presented in Fig. 3. Let us assume further that there are s links in the direction which can carry a class i call. Further assumption is that there are $d(i)$ last-stage switches available for the given first-stage switch. The internal point-to-group blocking phenomenon appears when all links (of the considered direction) belonging to the $d(i)$ available last-stage switches have not sufficient number of free BBUs for the class i call. Consequently, the point-to-group internal blocking probability E_i^{in} may be expressed as follows:

$$E_i^{in} = \sum_{s=1}^{k-d(i)} \frac{P_k(i,s)}{1-P_k(i,0)} \left[\binom{k-s}{d(i)} \Big/ \binom{k}{d(i)} \right], \tag{21}$$

where k is the total number of links in the direction, and $P_k(i,s)$ is the so-called distribution of available links in the direction. The distribution $P_k(i,s)$ determines the probability of an event in which each of arbitrarily chosen s links in the required direc-

tion can carry the class i call. In the proposed PGBMF method, the distribution $P_k(i,s)$ is approximated by distribution of available links $P_k(i,s)$ in the limited-availability group.

The phenomenon of the external blocking occurs when none of outgoing links of the demanded direction of the switching network can service the class i call (i.e. does not have t_i free BBUs). The occupancy distribution of the outgoing direction can be approximated by the distribution of available links in LAG with BPP traffic. Thus, the external blocking probability can be calculated by the formula:

$$E_i^{ex} = P(i,0). \tag{22}$$

The total blocking probability E_i for the class i call is determined by external and internal blocking probabilities. Assuming the independence of internal and external blocking events, we obtain:

$$E_i = E_i^{ex} + E_i^{in}[1 - E_i^{ex}]. \tag{23}$$

For blocking probability calculation E_i, it is necessary to determine the value of $d(i)$. The parameter $d(i)$ is known as the effective availability of the switching network for the class i call stream and will be described in Sect. 3.6.

3.3. POINT-TO-POINT BLOCKING FOR MULTI-RATE BPP TRAFFIC – PPBMF METHOD

Let us consider now the PPBMF method for blocking probability calculation in switching networks with point-to-point selection, servicing multi-rate BPP traffic. The basis for the proposed method is the PPBMT method (Point-to-Point Blocking for Multi-channel Traffic) worked out in [10] for switching networks with an infinite source populations. Modifications to the PPBMF method consists in the introduction of appropriate group models with traffic generated by a finite source population, determined in Section 2, to calculations. In the method, blocking probability calculations for the switching networks with point-to-point selection are made in accordance with Lotze's remark [30] that point-to-point blocking in z-stage switching network is equal to point-to-group blocking in a $(z-1)$-stage switching network. In such a system the incoming links to the switch of the last z-stage are considered to be an outgoing group (direction).

Let us assume that a certain switch β belonging to the last stage of the switching network, chosen by the control system, has t_i free BBUs necessary to set up the class i connection. We can also assume that for the switch α (on the incoming links of which there appears the class i call) there are $d_e(i)$ available interstage links coming to the destination switch β from the last but one stage. The internal point-to-point blocking phenomenon appears when none of the $d_e(i)$ available multiplexed links have a sufficient number of BBUs for servicing the class i call. In the light of the above consideration, the point-to-point blocking probability can be expressed by the formula:

$$E_i^{in} = \sum_{s=0}^{k-d_e(i)} P(i, s \wedge 1) \left[\binom{k-s}{d_e(i)} \Big/ \binom{k}{d_e(i)} \right], \tag{24}$$

where $P(i, s \wedge 1)$ is the so-called combinatorial distribution of available links in a switch, described by Equation (25) in the further part of the paper. The phenomenon of the external blocking occurs when none of outgoing links of the demanded direction of the switching network can service the class i call (i.e. does not have t_i free BBUs). The occupancy distribution of the outgoing direction can be approximated by the distribution of available subgroups (links) in the limited-availability group with BPP traffic. Thus the external blocking probability, and consequently, the total blocking probability, can be calculated by the formulae (22) and (23), respectively.

3.4. COMBINATORIAL DISTRIBUTION OF AVAILABLE LINKS IN A SWITCH

The probability of the internal point-to-point blocking for the class i call stream is calculated with the assumption that at least one incoming link and one outgoing link of the system have at least t_i free BBUs. The fact that one of the incoming links of the switch is available for the class i call does not mean simultaneously that one of its outgoing links is also available.

The probability of available links in a switch $P(i, s \wedge 1)$ was determined on the basis of conditional distribution (19) of available subgroups in the limited-availability group. This probability determines an event in which s incoming links and, at the same time, at least one of the outgoing links of a given switch (e.g. the switch β) are available for the class i call. According to the consideration worked out in [10], this distribution can be written as follows:

$$P(i, s \wedge 1) = \frac{\sum_{x=0}^{V} P(i, s|x)[1 - P(i, 0|x)][P_{V-x}]_V}{1 - \sum_{n=0}^{k} \left[\sum_{x=0}^{V} P(i, n|x) P(i, 0|x) [P_{V-x}]_V \right]}, \tag{25}$$

where $P(i, s|x)$ – conditional distribution of available links in LAG with BPP traffic, $[P_n]_V$ – occupancy distribution in LAG with BPP traffic.

3.5. POINT-TO-POINT BLOCKING FOR MULTI-RATE BPP TRAFFIC – PPFD METHOD

In the other of the proposed method of blocking probability calculation in switching networks with point-to-point selection and BPP traffic, the PPFD method, the evaluation of the internal point-to-point blocking probability is made on the basis of the effective availability quotient and the capacity of an outgoing group. The proposed method is based on the PPD method, elaborated in [12] for switching networks with an infinite source population.

In order to explain the basic assumptions of the proposed method, let us consider a switching network with point-to-point selection. An outgoing link belonging to a given last-stage switch is considered to be available for the first-stage switch if it is possible to set up a class i connection between these switches.

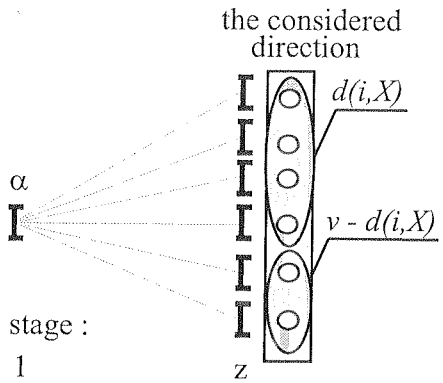

Fig. 4. Available and unavailable switches in a switching networks

Let us assume that the z-stage switching network is in a state X. The control system determines the first-stage switch, on the incoming link of which there appears a class i call (switch α). First, the control system finds the last-stage switch (switch β) having a free outgoing link in the demanded direction. Then, the control system tries to find a connection path for class i call between the switches α and β. Let us assume that in the state X there are $d(i, X)$ available last-stage switches for the switch α. If the chosen switch β belongs to the group of $d(i, X)$ available switches, then class i connection is set up, otherwise connection is lost because of the internal blocking event. Thus, the probability of the internal blocking can be determined as a ratio of free links belonging to an unavailable group of $V - d(i, X)$ switches to all free links in a given direction (Fig. 4). If we assume that the probability of links occupancy is the same for all links of the direction, the average value of internal blocking is equal to:

$$E_i^{in} = \sum_{\Omega} \frac{V - d(i,X)}{V} P(X), \tag{26}$$

where Ω is the set of all possible states X of a switching network and $P(X)$ is the state probability of a switching network. If we designate the average value of available last-stage switches by $d_e(i)$, Equation (26) can be finally rewritten as follows:

$$E_i^{in} = \frac{V - d_e(i)}{V}. \tag{27}$$

The phenomenon of external blocking occurs when none of outgoing links of the demanded direction in a switching network can service a class i call. The occupancy

distribution of the outgoing direction can be approximated by the occupancy distribution in the limited availability group. Consequently, the external blocking probability E_i^{ex} and the total blocking probability E_i for class i calls, can be calculated by the formulae (22) and (23), respectively.

3.6. EFFECTIVE AVAILABILITY

The concept of the so-called equivalent switching network [20] is the base for effective availability calculation for class i traffic stream. Following this concept, the network with multi-rate traffic is reduced to an equivalent network carrying a single-rate traffic. Each link of the equivalent network is treated as a single-channel link with a fictitious load $e_l(i)$ equal to blocking probability for a class i stream in a link of a real switching network between section l and $l + 1$. This probability can be calculated on the basis of the occupancy distribution in the full-availability group with BPP traffic streams (Sect. 2.4).

The effective availability in a real z-stage switching network is equal to the effective availability in an equivalent switching network and can be determined by the formula derived in [10]:

$$d(i) = [1 - \pi_z(i)]k + \pi_z(i)\eta Y_1(i) + \pi_z(i)[k - \eta Y_1(i)]e_z(i)\sigma_z(i), \tag{28}$$

where:

- $d(i)$ – the effective availability for the class i traffic stream in an equivalent network,
- $\pi_z(i)$ – the probability of non availability of a given last stage switch for the class i connection. $\pi_z(i)$ is the probability of an event where the class i connection path cannot be set up between a given first-stage switch and a given last-stage switch. Evaluation of this parameter is based on the channel graph of the equivalent switching network and can be calculated by the Lee method [31].
- k – the number of outgoing links from the first stage switch (Fig. 3),
- $Y_1(i)$ – the average value of the fictitious traffic served by the switch of the first stage:

$$Y_1(i) = ke_1(i), \tag{29}$$

- $e_c(i)$ – the blocking probability for the class i stream in an interstage link (between stages c and $c + 1$) of a real network. The $e_c(i)$ parameter can be calculated on the basis of the full-availability group model with multi-rate traffic
- η – a portion of the average fictitious traffic from the switch of the first stage which is carried by the direction in question. If the traffic is uniformly distributed between all h directions, we obtain:

$$\eta = 1/h, \tag{30}$$

- $\sigma_z(i)$ – the so-called secondary availability coefficient [10] which is the probability of an event in which the connection path of the class i connection passes through directly available switches of intermediate stages [10]:

$$\sigma_z(i) = 1 - \prod_{j=2}^{z-1} \pi_j(i). \tag{31}$$

In the description of $\sigma_z(i)$ we use the terms "direct available switch" and "direct availability". Following [10], a switch of stage l is directly available for the first-stage switch if it is possible to set up a connection between these switches. The term direct availability of stage l means the average number of directly available switches of stage l.

4. CALCULATION AND SIMULATION RESULTS

In order to confirm the adopted assumptions in the PGBMF, PPBMF and PPFD method, the results of the analytical calculations were compared with the simulation results of a 3-stage switching network. The structure of the switching network consisting of the switches of $k \times k$ links is shown in Fig. 3. The results presented in the paper (Figs. 5–13) were obtained for the switching network with the parameters: $k = 4, f = 30, t_1 = 1, t_2 = 2, t_3 = 6$. The research was carried out for different values of the ratio of the number of traffic sources (Pascal and Engset traffic streams) of all classes and the switching network capacity. The results of the simulation are shown in the charts in the form of marks with 95% confidence intervals that have been calculated according to the t-Student distribution for the five series with 1,000,000 calls of this traffic class that generates the lowest number of calls. For each of the points of the simulation, the value of the confidence interval is at least one order lower than the mean value of the results of the simulation. In many a case, the value of the confidence interval is lower than the height of the sign used to indicate the value of the simulation experiment. All the results are expressed in relation to the value of total traffic offered to a single BBU at the entry to the network.

Figures 5, 6 and 7 show the results of point-to-group and point-to-point blocking probability in the switching network with an infinite source population. The results obtained allow us to compare the accuracy of the model of the switching network with an infinite population of traffic sources with the accuracy of the proposed calculation methods in the case of the switching network with a finite source population, both for Engset (Figs. 8, 9, 10) and Pascal traffic streams (Figs. 11, 12, 13). We can notice that the proposed methods of blocking probability calculation in switching networks with BPP traffic ensures high accuracy.

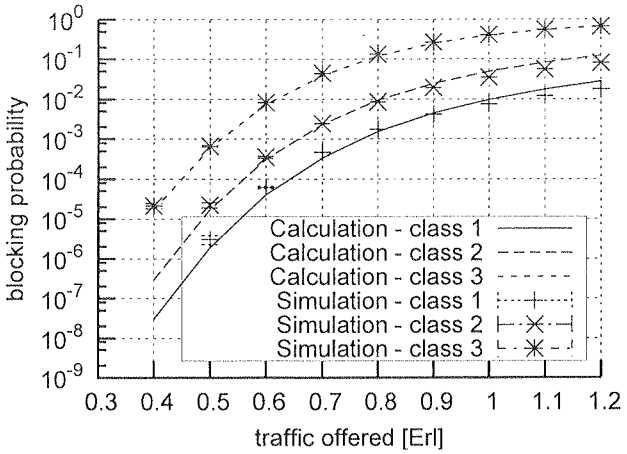

Fig. 5. Point-to-group blocking probability in the switching network with Erlang traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, PGBMT method [10]

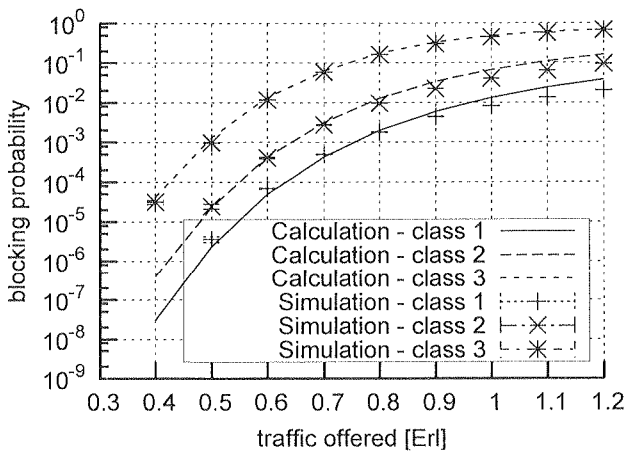

Fig. 6. Point-to-point blocking probability in the switching network with Erlang traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, PPBMT method [10]

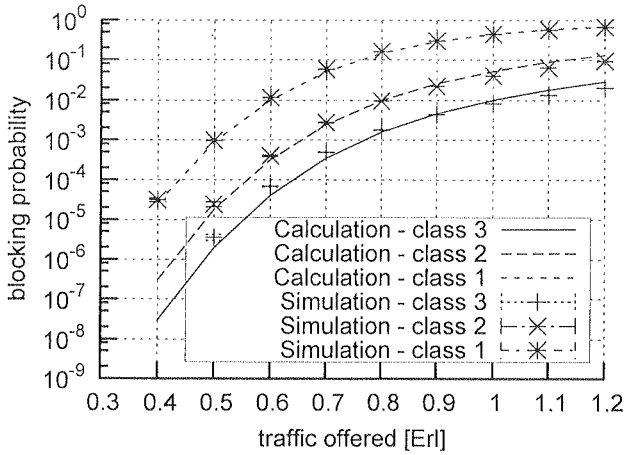

Fig. 7. Point-to-point blocking probability in the switching network with Erlang traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, PPD method [12]

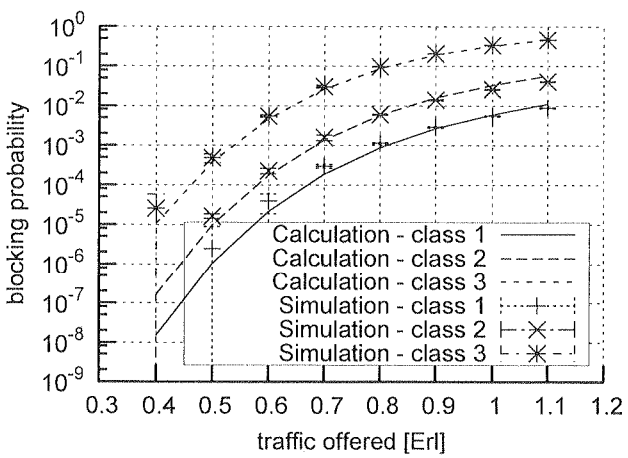

Fig. 8. Point-to-group blocking probability in the switching network with Engset traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $N_1 = N_2 = N_3 = 400$, PGBMF method

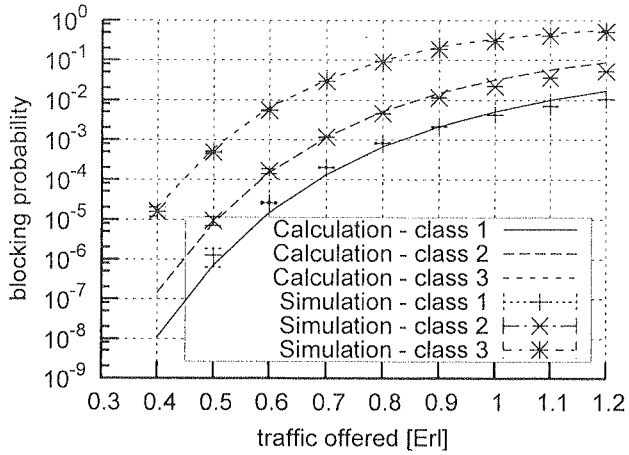

Fig. 9. Point-to-point blocking probability in the switching network with Engset traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $N_1 = N_2 = N_3 = 800$, PPBMF method

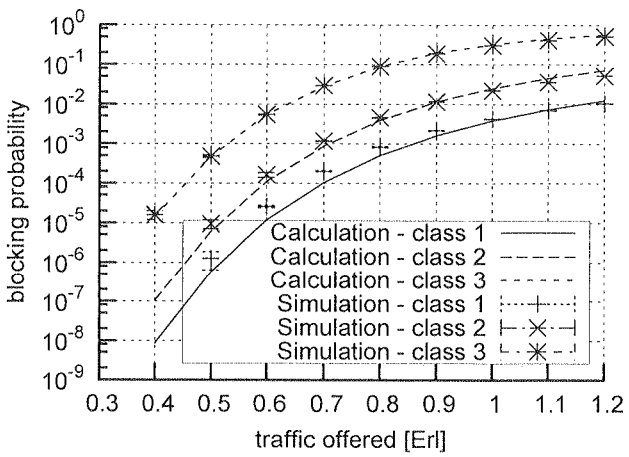

Fig. 10. Point-to-point blocking probability in the switching network with Engset traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $N_1 = N_2 = N_3 = 800$, PPFD method

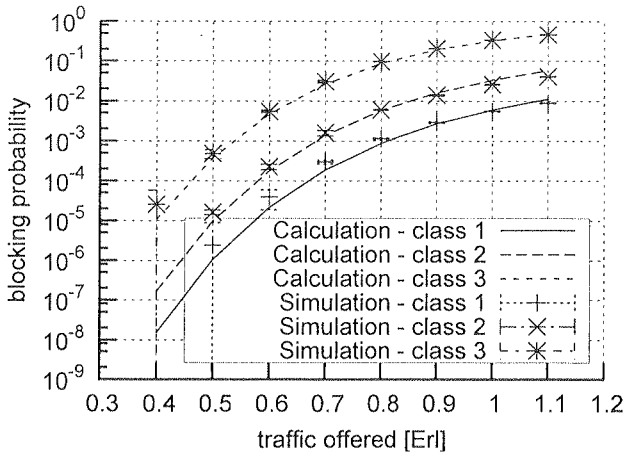

Fig. 11. Point-to-group blocking probability in the switching network with Pascal traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $S_1 = S_2 = S_3 = 320$, PGBMF method

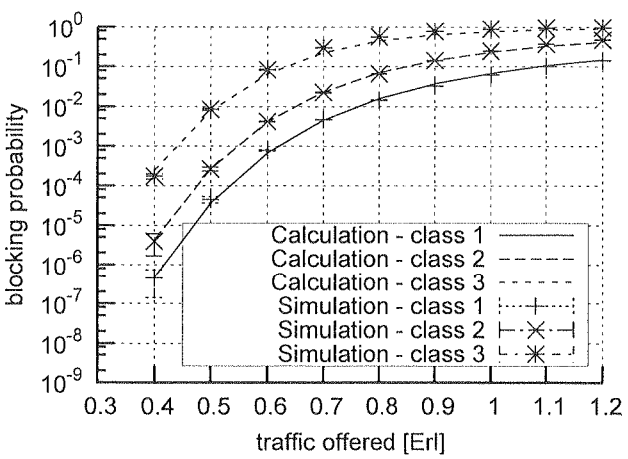

Fig. 12. Point-to-point blocking probability in the switching network with Pascal traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $S_1 = S_2 = S_3 = 320$, PPBMF method

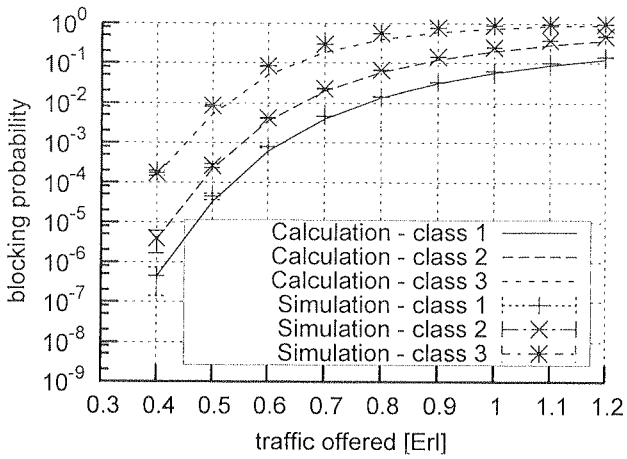

Fig. 13. Point-to-point blocking probability in the switching network with Pascal traffic streams, $A_1t_1 : A_2t_2 : A_3t_3 = 1 : 1 : 1$, $S_1 = S_2 = S_3 = 320$, PPFD method

5. CONCLUSIONS

The paper presents the approximate methods of point-to-group and point-to-point blocking probability calculation in switching networks with multi-rate traffic generated by Binomial, Poisson and Pascal traffic sources (BPP traffic). The method is based on the concept of effective availability. The analytical results of blocking probability, obtained on the basis of the proposed methods, are compared with the simulation results. The simulation results confirm high accuracy of the proposed analytical models. Due to the limited space available in the paper, we have restricted ourselves to present only the selected results. However, numerous simulation experiments indicate that similar accuracy of the proposed analytical model can be obtained for various structures of switching networks and for various number of traffic classes.

6. REFERENCES

1. H. Akimuru, K. Kawashima: *Teletraffic: Theory and Application.* Springer, Berlin-Heidelberg New York, 1999.
2. J. W. Roberts, V. Mocci, I. Virtamo, editors: Broadband Network Tele-traffic, Final Report of Action COST 242. Commission of the European Communities, Springer, Berlin, 1996.
3. K. W. Ross: *Multiservice Loss Models for Broadband Telecommunication Network.* Springer, London, 1995.
4. W. Bziuk: *Approximate state probabilities in large shared multi-rate loss systems with an application to trunk reservation.* 2nd Polish-German Teletraffic Symposium, pp. 145-152, Gdańsk, Poland, 2002.

5. I. D. Moscholios, M. D. Logothetis, G. K. Kokkinakis: *Connection-dependent threshold model: a generalization of the Erlang multiple rate loss model.* J. Perf. Eval, Vol. 48, No. 1-4, pp. 177-200, 2002.
6. V. B. Iversen, editor: *Teletraffic Engineering Handbook.* ITU-D, Study Group 2, Question 16/2, Geneva, December 2003.
7. J. W. Roberts, editor: *Performance Evaluation and Design of Multiservice Networks, Final Report COST 224.* Commission of the European Communities, Brussels, 1992.
8. J. Conradt, A. Buchheister: *Considerations on loss probability of multi-slot connections.* 11th Int. Teletraffic Congress, paper. 4.4B-2.1, Kyoto, 1985.
9. M. E. Beshai, D. R. Manfield: *Multichannel services performance of switching networks.* 12th Int. Teletraffic Congress, pp. 857-864, Torino, 1988.
10. M. Stasiak: *Combinatorial considerations for switching systems carrying multi-channel traffic streams.* Annales des Télécommunications, vol. 51, No. 11-12, pp. 611-625, 1996.
11. M. Stasiak, M. Głąbowski: *PPBMR method of blocking probability calcu-lation in switching networks with reservation.* GLOBECOM 1999, Vol.1a, pp. 32-36, Rio de Janeiro, 1999.
12. M. Stasiak, M. Głąbowski: *Point-to-point blocking probability in switching networks with reservation.* 16th Int. Teletraffic Congress, vol. 3A, pp. 519-528, Edinburgh, 1999.
13. M. Głąbowski, M. Stasiak: *Point-to-point blocking probability in switching networks with reservation.* Annales des Télécommunications, vol. 57, No. 7-8, pp. 798-831, 2002.
14. M. Stasiak, M. Głąbowski: *Multi-service switching networks with point-to-group selection and several attempts of setting up a connection.* 1st Int. Working Conference on Performance Modelling and Evaluation of Heterogeneous Networks, pp. 1/1-1/12, Ilkley, 2003.
15. V. B. Iversen: *The exact evaluation of multi-service loss systems with access control.* In Seventh Nordic Teletraffic Seminar, pp. 56-61, Lund, 1987.
16. J. S. Kaufman: *Blocking in a shared resource environment.* IEEE Transactions on Communications, Vol. 29, No. 10., pp. 1474-1481, 1981.
17. J. W. Roberts: *A service system with heterogeneous user requirements – application to multi-service telecommunications systems.* Performance of Data Communications Systems and their Applications, pp. 423-431, Amsterdam, 1981.
18. A. Lotze, A. Roder, G. Thierer: *PPL – a reliable method for the calculation of point-to-point loss in link systems.* 8th Int. Teletraffic Congress, pp. 547/1-44, Melbourne, 1976.
19. E. B. Ershova, V. A. Ershov: *Digital Systems for Information Distribution.* Radio and Communications, Moscow, 1983. in Russian.
20. M. Stasiak: *Blocage interne point a point dans les reseaux de connexion.* Annales des Télécommunications, vol. 43, No. 9-10, pp. 561-575, 1988.
21. Y. Kogan, M. Shenfild: *Asymptotic solution of generalized multiclass Engset model.* 14th Int. Teletraffic Congress, volume 1b, pp. 1239-1249, Antibes Juan-les-Pins, 1994.
22. G. L. Choudhury, K. K. Leung, W. Whitt: *An inversion algorithm to compute blocking probabilities in loss networks with state-dependent rates.* IEEE/ACM Trans. Networking, Vol. 3, No. 5, pp. 585-601, 1995.
23. S. A. Berezner, A. E. Krzesinski: *An efficient stable recursion to compute multiservice blocking probabilities.* J. Perf. Eval., Vol. 43, No. 2-3, pp. 151-164, 2001.
24. G. M. Stamatelos, J. F. Hayes: *Admission-control technics with application to broadband networks.* Computer Communication, Vol. 17, No. 9, pp. 663-673, 1994.
25. D. P. Heyman, T. V. Lakshman, A. L. Neidhardt: *A new method for ana-lyzing feedback based protocols with applications to engineering Web traffic over the Internet.* Computer Communications, Vol. 26, No. 8, pp. 785-803, 2003.
26. M. Ermel, et al.: *Performance of GSM networks with general packet radio services.* J. Perf. Eval., Vol. 48, No. 1-4, pp. 285-310, 2002.

27. M. Głąbowski: *Blocking probability in multi-service switching networks with finite source population.* The 14th IEEE Int. Conference On Telecommunications, Penang, 2007.
28. M. Głąbowski: *Point-to-Point Blocking Probability Calculation in Multi-service Switching Networks with BPP Traffic.* The 14th Polish Teletraffic Symposium, Zakopane, September 2007, pp. 65-76.
29. M. Stasiak, M. Głąbowski: *A simple approximation of the link model with reservation by a one-dimensional Markov chain.* J.Perf. Eval., Vol. 41, No. 2-3, pp. 195-208, 2000.
30. A. Lotze, A. Roder, G. Thierer: *Point-to-point selection versus point-to-group selection in link systems.* 8th Int. Teletraffic Congress, pp. 541/1-5, Melbourne, 1976.
31. C. Lee: *Analysis of switching networks.* BSTJ, Vol. 34, No. 6, 1955.
32. A. Lotze: *Loss formula, artificial traffic check and quality standards for characterizing one stage gradings.* 3th Int. Teletraffic Congress, paper 28, Paris, 1961.
33. A. D. Charkiewicz: *An approximate method for calculating the number of junctions in a crossbar system exchange.* Elektrosvyaz, No. 2, pp. 55-63, 1959.

A low-power strategy for Delta-Sigma modulators

SERGIO PESENTI[1], DANICA STEFANOVIC[1], PATRICK CLEMENT[1], MAHER KAYAL[2]

[1] *Marvell Semiconductor, Route de Pallatex 17, 1163 Etoy, Switzerland,*
spesenti@marvell.com
[2] *LEG Electronics Laboratory, EPFL Ecole Polytechnique Fédérale de Lausanne,*
Station 11, 1015 Lausanne, Switzerland,
maher.kayal@epfl.ch

Received 2007.09.24
Authorized 2007.11.05

This paper presents a hybrid continuous-discrete-time Delta-Sigma modulator for portable communication systems following a low-power strategy. The proposed design methodology is extendable to different specifications. A multi-bit technique has been introduced in an efficient manner to optimize the power consumption, and an adaptive algorithm is used to allow a 3-fold reduction in the number of comparators.

Keywords: Hybrid Delta-Sigma modulator, auto-ranging algorithm, multi-bit feedback, mismatch shaping encoder

1. INTRODUCTION

Delta-Sigma Modulators (DSMs) are widely used for Analog-to-Digital Conversion (ADC) in both the audio and the radio communication areas. To comply with stringent specifications of power consumption and performance, their implementation is often a combination of different techniques, each of them having its own limitations. In this paper a 0.18 μm CMOS technology has been used to design a Delta-Sigma Modulator. A low-power design methodology is proposed in order to extend this implementation toward a typical case of a wireless portable application.

2. LOW-POWER STRATEGY

Fig. 1 describes the main blocks and design procedures of this modulator. The main target of this work is based on low power techniques. The following approaches have been applied:

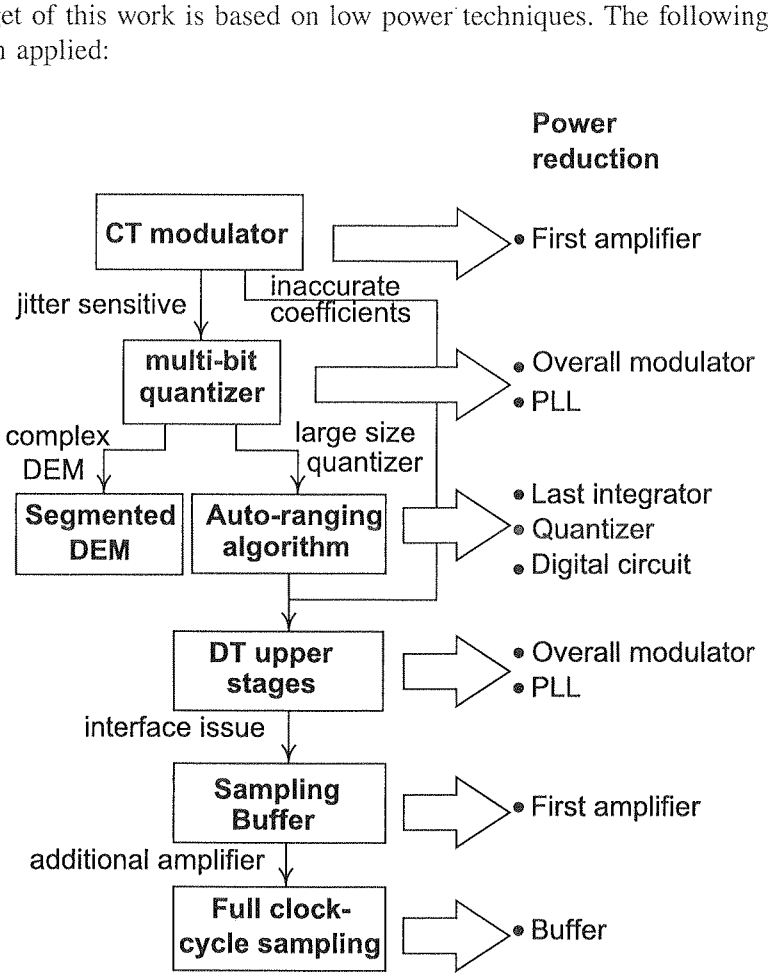

Fig. 1. Low-power design strategy

- The input stage amplifier is working in a Continuous-Time (CT) to lower the first integrator consumption.
- The clock jitter issue brought by the CT implementation is mitigated by increasing the internal Number of Levels (NL).
- The Number of Comparators is reduced by an Auto-Ranging (AR) algorithm [1][2][3][4].

- The complexity of the digital mismatch shaping encoder, also referred to as Dynamic Element Matching (DEM), is lowered by an appropriate segmentation of a tree structure [5].
- Since both high-order modulators and the auto-ranging algorithm require an accurate control of the last feedback coefficient, the upper stages are kept in a discrete-time implementation.
- Multi-bit discrete-time implementation allow a more aggressive quantization noise shaping and therefore allow a lower sampling frequency, reducing therefore the consumption of the overall modulator.
- The continuous-time and discrete-time stages are isolated by a buffer whose consumption is reduced by a full clock-cycle sampling scheme.

2.1. HYBRID CONTINUOUS-DISCRETE-TIME IMPLEMENTATION

In a low-pass Delta-Sigma Modulator each successive stage, starting with the second one, benefits from the order error shaping provided by the previous stages. For this reason, a significant part of the power consumption takes place in the first stage.

Continuous-time implementations consume less current than their Switched-Capacitor (SC) counterpart [6][7]. On the other hand, SC circuits offer an accurate control of the filter parameters without tuning, which is essential to provide a very aggressive quantization noise shaping. Fig. 2 shows the tolerance of the first and last loop

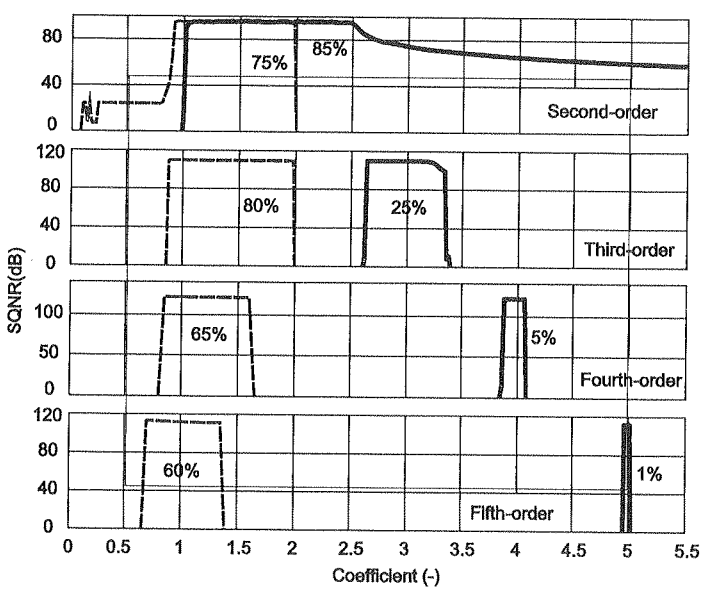

Fig. 2. First (dashed) and last coefficients tolerance for a low-pass multi-path feedback modulator of the second, third, fourth and fifth-order

coefficients for a low-pass modulator in a multi-path feedback topology. The plots shows that the higher the order, the narrower the tolerance on the last coefficient. In contrast, the first coefficient tolerance remains quite large. Furthermore, high-order modulators often include local feedbacks, providing an optimal distribution of the Noise Transfer-Function (NTF) zeros, with coefficients that are usually very small and also need an accurate control.

A hybrid architecture, such as proposed in [8][9][10], is implemented here where only the first integrator is a CT, with a No-Return-to-Zero (NRZ) feedback. Fig.3(a) describes the second-order hybrid modulator we have designed with the characteristics of Tab.1.

Table 1

System characteristics

Internal quantizer	11 levels
Emulated quantizer	33 levels
Sampling frequency	32 MHz
Bandwidth	500 kHz
OSR	32
SQNR	93.8 dB
SNDR target	83.0 dB
Supply voltage	1.8 V
CMOS technology	0.18 um
Input amplitude	500 mVpk,diff

According to Fig. 2, the second-order architecture does not require much accuracy, but the implementation is intended to be extendable to higher orders. Fig. 4 shows an equivalent DT block diagram. The modulator has been designed with an NTF with two poles in the center of the complex unity circle and two zeros at DC. In such a case, the maximum Signal-to-Quantization-Noise Ratio (SQNR) as a function of the Over-Sampling Ratio (OSR) is given by

$$\mathrm{SQNR}_{\max} = \frac{3}{2}\pi(2n+1)\left(\frac{\mathrm{OSR}}{\pi}\right)^{2n+1}(\mathrm{NL}-2^n+1)^2 \qquad (1)$$

where n is the modulator order, here equal to 2, and NL the internal Number-of-Levels.

The transition from Continuous to discrete-time domain is performed by a full-clock-cycle-sampling scheme, using two sets of capacitors. A unity-gain buffer is necessary to guarantee the proper CT operation of the first amplifier. The tasks of CT integration and sampling are separated. This is an efficient way of maintaining low power consumption in the first amplifier.

2.2. FULL CLOCK-CYCLE SAMPLING

As shown in Fig. 3(a) and according to the clocking diagram of Fig. 3(b), two sets of differential capacitors are used alternatively allowing the sampling to start during the integration phase of the second-stage. The sampling phase lasts two halves of clock-cycle and twice as much time is given to the unity-gain buffer to settle.

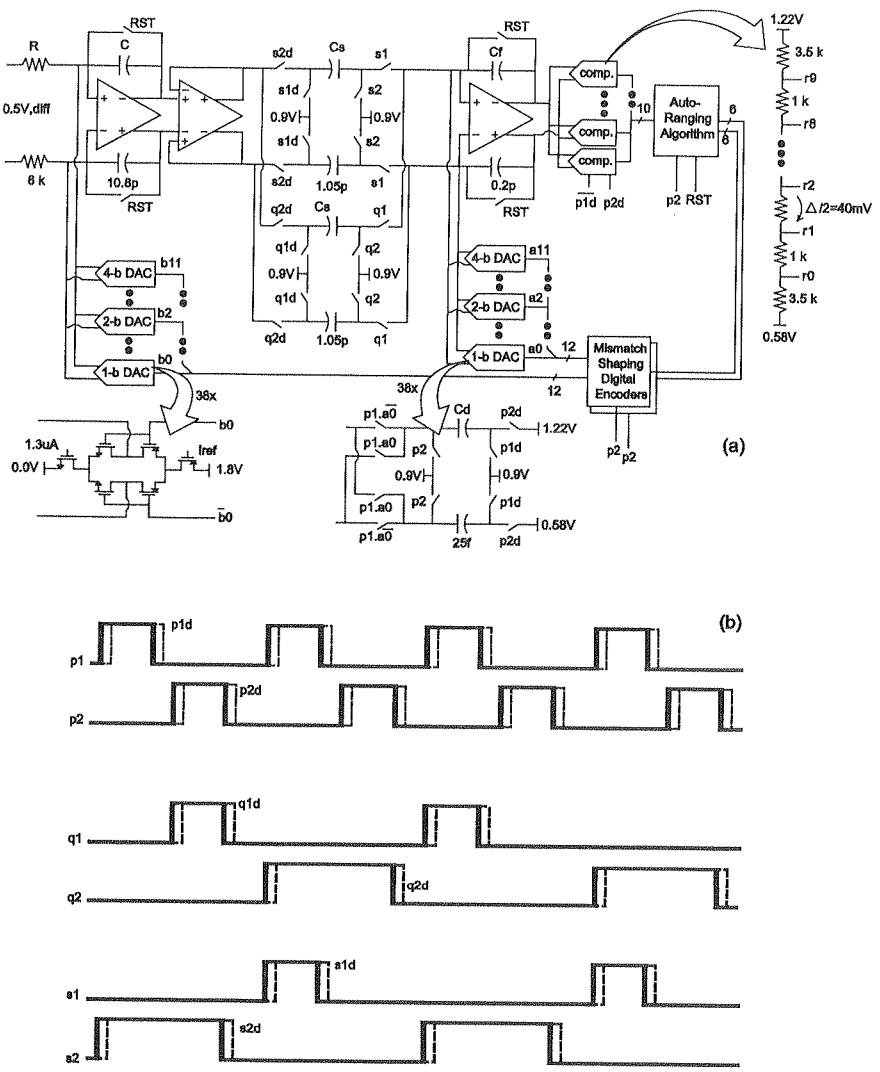

Fig. 3. 33-level second-order low-pass hybrid CT-DT modulator (a) and its clocking diagram (b)

The mismatch between the two sets of capacitors turns into a modulation of the signal at the output of the first stage F(z) which has a Power Spectral Density (PSD) PF(f).

$$P_F = \left|1 - z^{-1}\right|^2 \cdot \frac{\Delta^2}{12 f_s} \cdot \left(\frac{C_f}{C_s}\right)^2 \tag{2}$$

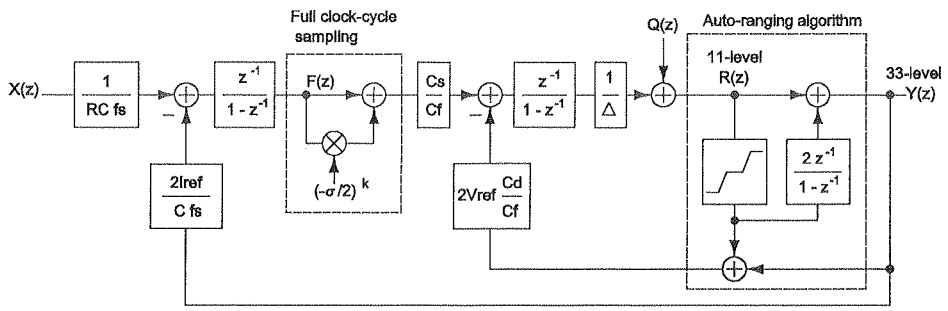

Fig. 4. Equivalent discrete-time block diagram

As modeled in the equivalent discrete-time diagram of Fig. 4, the signal splits into a direct path and a modulation [11] by (-sigma/2)^k, where sigma is the mismatch between the sets of capacitors and k the discrete time-steps. As a first approximation, this is equivalent to adding at that node a shifted version of PSD of F(f), weighted by the power of the modulating signal. The error signal is further shaped by the modulator before reaching the output with a PSD of M(f). Besides, the quantization noise PSD of Q(f) at the modulator output is known. We can therefore write

$$P_M = \frac{1}{12 f_s} \cdot \frac{\sigma^2}{4} \cdot \left|\left(1 - z^{-1}\right)\left(1 + z^{-1}\right)\right|^2 \tag{3}$$

$$P_Q = \frac{1}{12 f_s} \cdot \left|\left(1 - z^{-1}\right)^2\right|^2 \tag{4}$$

The degraded SNR can be evaluated by integrating the PSDs over the band of interest fb.

$$SNR = \frac{SQNR}{1 + \frac{\sigma^2}{4} \cdot \frac{\int_0^{f_b} \left|\left(1 - z^{-1}\right)\left(1 + z^{-1}\right)\right|^2 df}{\int_0^{f_b} \left|\left(1 - z^{-1}\right)^2\right|^2 df}} \tag{5}$$

Considering an OSR>>1, this relationship becomes a simple function of the OSR and σ.

$$SNR = \frac{SQNR}{1 + \frac{5\sigma^2}{4} \cdot \left(\frac{OSR}{\pi}\right)^2} \tag{6}$$

As plotted in Fig. 5(f), Eq. 6 perfectly predicts the degradation except with a Full-Scale (FS) input signal. Highlighted by the power spectral densities of Fig. 5(c) and (d), the input signal modulated by the alternation folds around fs/2. This causes the modulator to overload with a FS input signal resulting in harmonic distortion, causing the SNR to drop prematurely. Fig. 5(c) shows the predicted folding and shaping of the quantization noise.

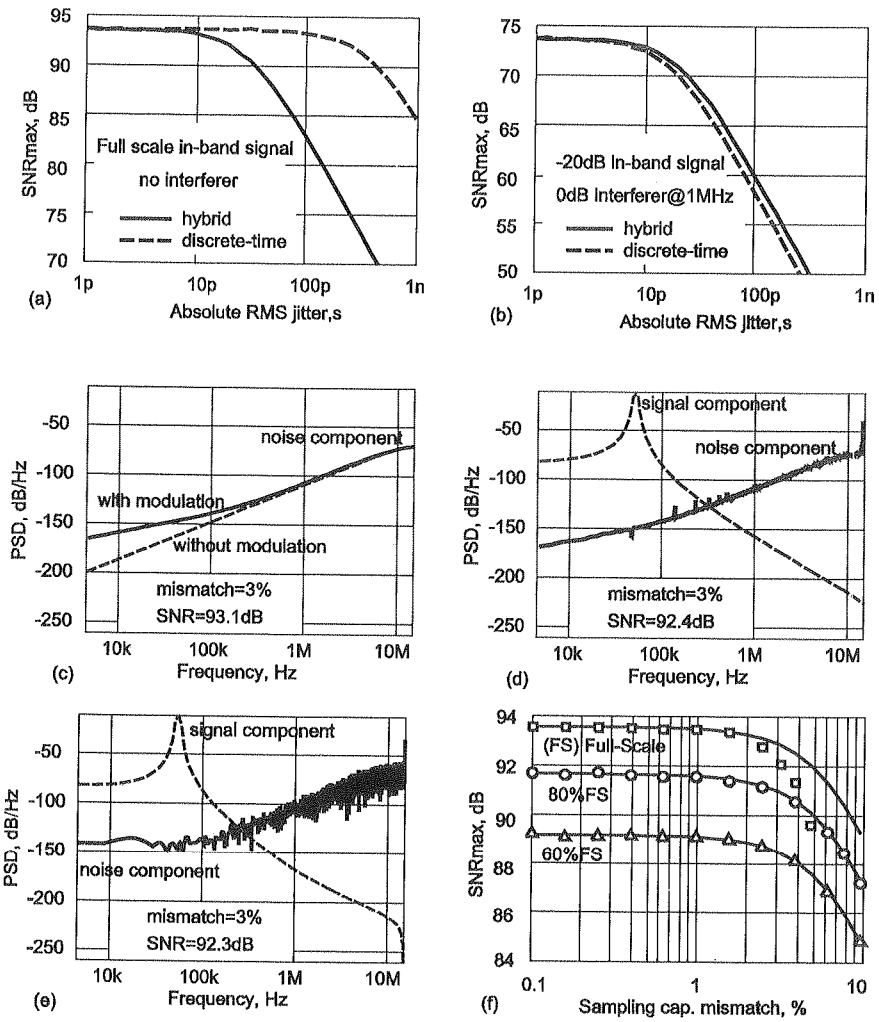

Fig. 5. Compared jitter sensitivities for hybrid and pure discrete-time modulator, with a full-scale in-band input signal (a) and with a-20 dB in-band signal and an additional full-scale out-of-band interferer at 1 MHz. Output PSD with a full-scale in-band signal and 3% sampling capacitors mismatch calculated (c), simulated with MATLAB (d) and with Verilog-A circuit-description (e). Sampling capacitors mismatch sensitivity simulated with MATLAB (f) with the curves provided by Eq. 6

In pure SC implementations, the sampling device would be placed in front of the modulator, not taking any advantage of this error shaping mechanism. In such a case, full clock-cycle sampling would be impractical and the settling accuracy more stringent, having a double impact on consumption.

3. MULTI-BIT FEEDBACK

The multi-bit technique reduces the voltage steps, which is essential for the clock jitter sensitivity of the CT stage. At the same time, for a given SQNR target, more internal levels bring the benefits of reducing the sampling frequency. This is essential to lower the current dissipated not only in the SC stage, but also in the digital circuits. Moreover, a lower frequency reduces the jitter sensitivity of the CT part. In CT implementations the dominant jitter issue is related to the feedback DAC step size, sampling errors being shaped by the modulator. On the contrary, a pure DT modulator is affected only by sampling errors occurring at the modulator input that depend on the signal amplitude-frequency product. Fig. 5(a) shows that a pure DT modulator is ten times less sensitive to clock jitter in our case. Nevertheless, according to Fig. 5(b), in presence of a large out-of-band interferer, the pure DT implementation is similarly affected in the hybrid structure.

3.1. CLOCK JITTER ANALYSIS

By inverting Eq. 1 we can express the OSR necessary to reach a targeted SQNR as

$$\mathrm{OSR} = \pi \left(\sqrt[2n+1]{\frac{2\ \mathrm{SQNR}_{\max}}{3\pi(2n+1)(\mathrm{NL}-2^n+1)^2}} \right) \tag{7}$$

The SQNR is usually determined by the converter required resolution and the modulator order n depends on the architecture choice. To any value of NL is associated a value of OSR, required to reach the SQNR. Thus, the set of NL and OSR form the design solutions. As shown in [12], relative clock jitter sigma providing a degradation of 3dB with respect to the SQNR is given by

$$\sigma_{3\mathrm{dB}} = \frac{1}{\xi}\sqrt{\frac{\mathrm{OSR}}{\mathrm{SQNR}}} \tag{8}$$

where xi is the jitter transfer factor calculated as

$$\xi = \sqrt{\left|\frac{(1-\exp[-j2\pi f/f_s])^{c+1}}{(j2\pi f/f_s)^c}\right|^2 + \frac{2}{3}\cdot\frac{(2n+2)!/(n+1)!^2}{(\mathrm{NL}-2^n+1)^2}} \tag{9}$$

The parameter c is number of continuous-time integration stage. The variables f and fs are the input signal and sampling frequency respectively.

The sensitivity to the relative clock jitter is traced in Fig. 6 for a targeted SQNR of 94 dB and different modulator orders. A full-scale out-of-band signal at a frequency fmax that is twice the band-of-interest fb is considered. The curves reveal an optimal solution set of {NL, OSR}. For the second-order architecture chosen in this design the highest efficiency is found at NL = 33 and OSR = 32.

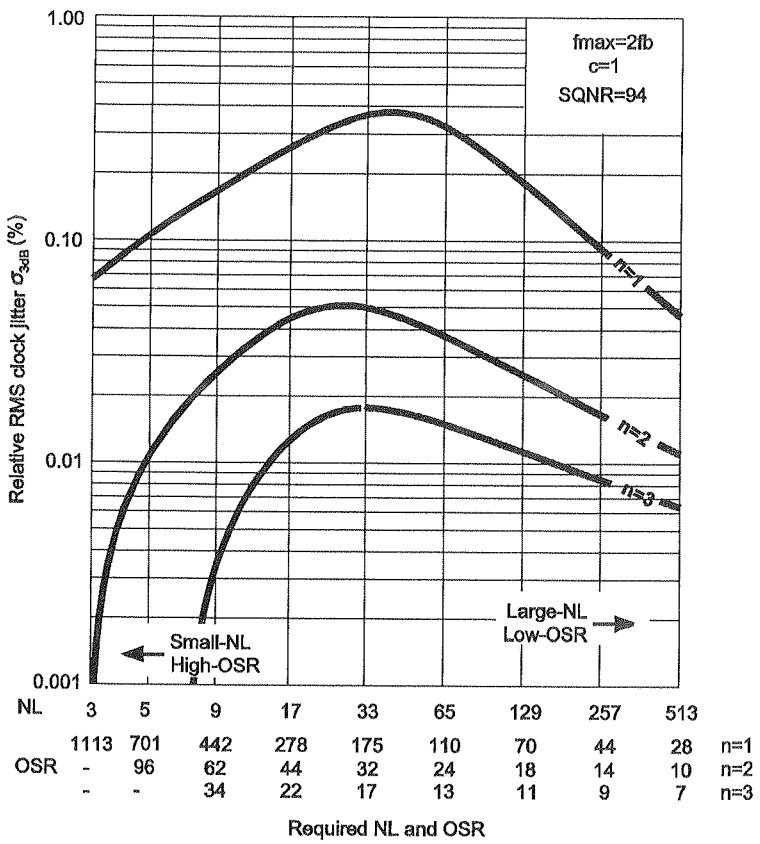

Fig. 6. Calculated sensitivity to relative jitter as a function of the set of parameters NL and OSR providing 94 dB of SQNR for different modulator orders

4. AUTO-RANGING ALGORITHM

The auto-ranging technique presented in [4] is an adaptive algorithm allowing to emulate, in this design, 33 internal levels with only 10 comparators. This is an extension of the technique used in 2 such that it can apply to higher-order multi-bit

modulators and sustain large out-of-band signals which are common in DSMs dedicated to communication receivers.

The algorithm is represented in the equivalent DT block diagram of Fig. 4 by a non-linear block and a feed-forward digital path matching the behavior of the last feedback of the DSM.

4.1. ALGORITHM PRINCIPLES

Based on the output of the 11-level quantizer R(z), the algorithm generates a control signal corresponding to a shift to be applied at both the input and output of the quantizer. The analog shift at the quantizer input is provided by the last feedback path whose loop gain was by design set to 2. The digital shift at the quantizer output is provided by a register and an adder. Both paths perform exactly the same operation such that the shifts are the same. This way of reusing the last integrator to make accurate analog shifts, reinforces the necessity of an SC stage as the last one. The algorithm generates shifts proportional to the quantizer output such as to maintain the quantizer output always in the center of its 11-level window. Its purpose is to track the slow-varying high-range input signal. The auto-ranging loop is not be sensitive to the fast-varying small-range quantization noise. For that reason, no shift is generated for the tree mid-range quantizer output. Neither does it generate a shift as the modulator output reaches the edges of the 33-level emulated window.

4.2. OPTIMAL EFFICIENCY

It is shown in [4] that the minimal reduced number of level NR is given by

$$NR_{min} = 2\gamma_{max} - 1 \tag{10}$$

where gamma is the number of step-changes seen by the quantizer at each clock cycle. The maximum of gamma is calculated as

$$\gamma_{max} = (NL - 2^n + 1)\sin\left[\frac{\pi}{2OSR}\right] + 2^n - 1 \tag{11}$$

for an nth-order NTF with all the poles placed in the center of the z-plan and all the zeros at DC. The efficiency of the algorithm can be evaluated by the ratio between the internal number-of-levels NL, emulated by the algorithm, and the minimum number-of-levels in the quantizer NRmin. In order to be conservative, we consider the presence of a full-scale out-of-band input signal at twice the band-of-interest. We therefore halve the OSR in Eq.11. Then, by inserting Eq.7 in Eq.10 we find the closed-form efficiency ratio

$$NL/NR_{min} = \frac{NL/2}{(NL - 2^n + 1)\sin\left[\sqrt[2n+1]{\frac{3\pi(2n+1)(NL-2^n+1)}{2SQNR}}\right] + 2^n - 1.5} \quad (12)$$

This expression is traced in Fig. 7 for a 94 dB of SQNR and different modulator orders. As in the analysis of the sensitivity of clock jitter, the curves reveal an optimal solution set of {NL, OSR}. Again, for the second-order architecture chosen in this design the highest efficiency is found at NL = 33 and OSR = 32.

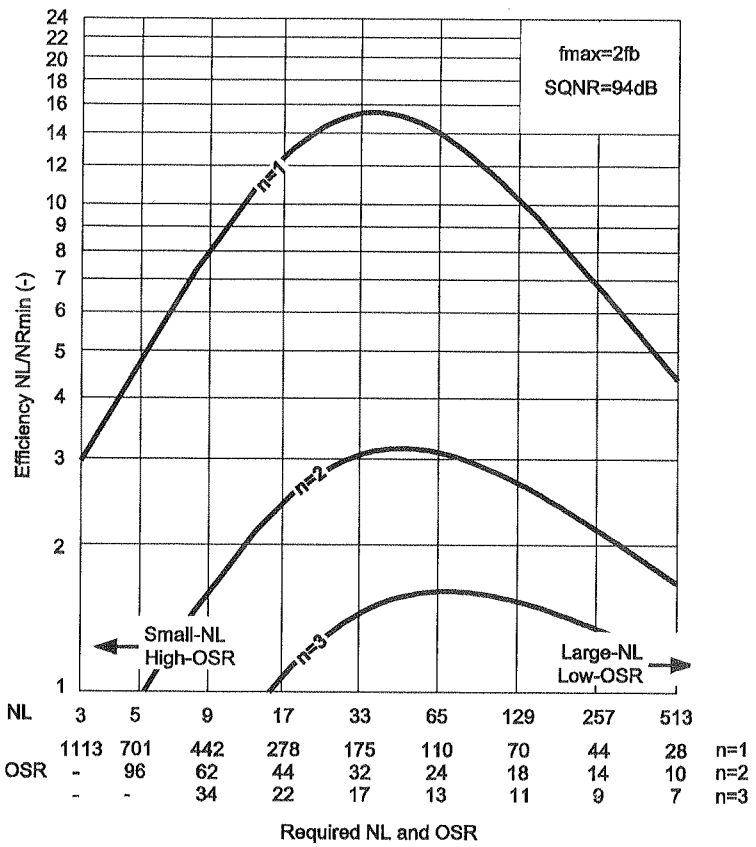

Fig. 7. Calculated algorithm efficiency as a function of the set of parameters NL and OSR providing 94 dB of SQNR for different modulator orders

Fig. 8 shows the maximum input signal amplitude supported by the algorithm with different reduced number-of-level in the quantizer. In this design with 10 comparators NR = 11 and the algorithm can sustain up to 1 MHz full-scale signals without any degradation of the modulator resolution. Faster out-of-band interferers need to be attenuated by the anti-aliasing filter.

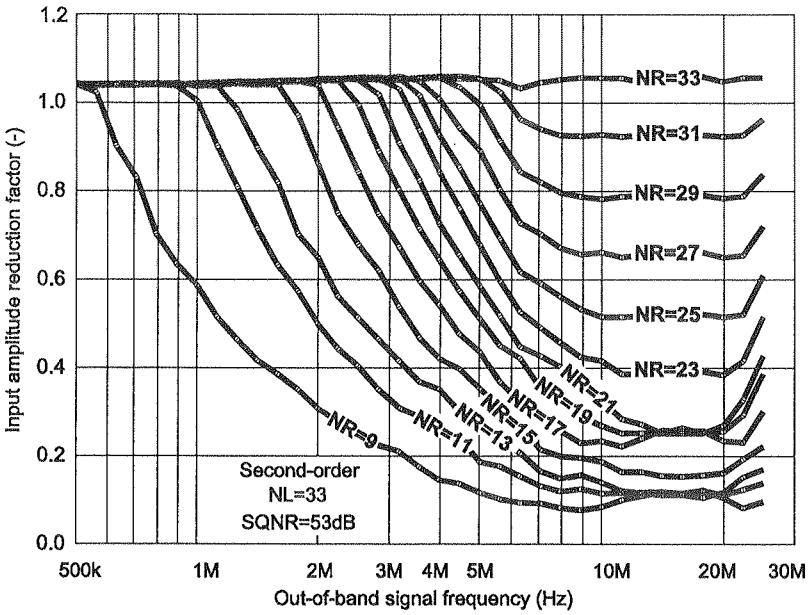

Fig. 8. Simulation results for a 33-level second-order modulator with different reduced number-of-levels NR. In this experiment, an in-band signal 40 dB bellow full-scale is applied together with a full-scale out-of-band at different frequencies. The curves show the out-of-band signal amplitude reduction necessary to prevent the modulator from overloading and to maintain an SQNR of 53 dB

Reducing NR significantly alleviates the capacitive load on the last stage. In this design, the load was further decreased by a small input differential pair size in the comparators. This results in large statistical comparator offsets. A 6-bit digital compensation developed by [13][14][15] is used for each comparator. The cost in terms of area and power are negligible. The compensation algorithm is activated only occasionally, without need to interrupting the modulator operations. Its disturbance is therefore imperceptible.

5. OPTIMAL ENCODER SEGMENTATION

The auto-ranging allowed increasing NL to 33 without the drawbacks of a large quantizer. However, the hardware complexity of the mismatch shaping encoder, here a tree-structured architecture, has grown exponentially. Additionally, using small DAC elements of 25 fF lead us towards a second-order shaping, further increasing this complexity.

Even though segmenting the encoder, as proposed in [4], drastically reduces the number of switching blocks, the total number of DAC elements increases, each DAC element representing an additional current and thermal noise source.

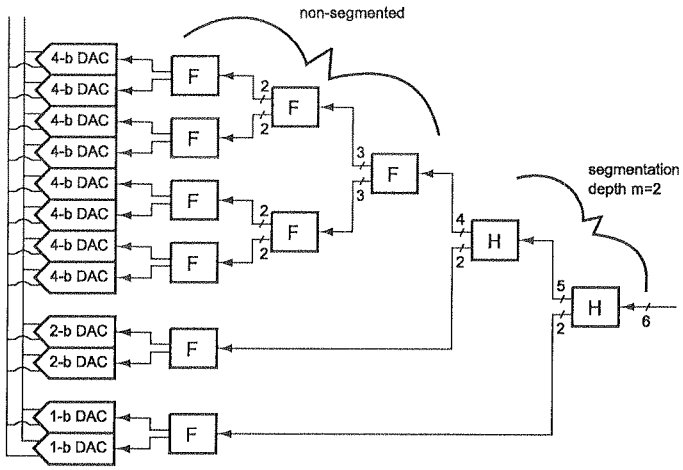

Fig. 9. Tree-structured encoder with standard segmentation

Using functional programming we generated all the 628 possible combinations considering the Quartering, Halving and Full switching blocks, referred to as Q, H and F blocks. Fig. 10 shows these structures classified according to the number of DAC elements and the total current consumption I. The curve links what we call here the standard segmentation solutions as described in Fig. 7, where only H and F blocks are considered. It can be shown that for a standard segmentation the analytical expression of I is given by

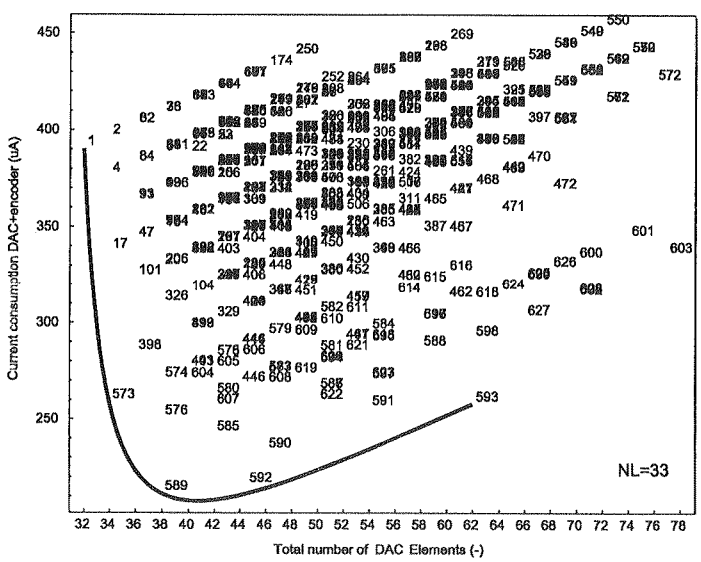

Fig. 10. Synthesized 628 segmented encoder structures for a 33-level DAC, classified with respect to the total current consumption and the number of DAC unit elements

$$I = (2^N + 2^{m+1} - 2)D + (2^{N-m} + m - 1)F + (m)H \quad (13)$$

where N and m are the encoder and segmentation depth respectively. H and F are the power consumption of the two different switching blocks and D the consumption of a DAC element. An optimal m value can be found, which provides the best solution in terms of power consumption. In our case a depth of 2 was chosen giving a total of 38 elements.

6. CONCLUSION

Following this optimization strategy, we came up with a transistor-level design that consumes 3.2 mA at 1.8 V, providing a Figure-Of-Merit (FOM), defined as FOM = Power/ (2^ENOB×Bandwidth), of 1.0 pJ. The ENOB is calculated based on the peak SNDR. Tab. 2 provides a comparison with the other previously published hybrid architectures. Fig. 11 shows the simulated PSD at transistor-level with an achieved SNR of 90 dB, very close to the ideal SQNR of 93.7 dB. The remaining degradation down to the target of 83 dB is left by design for thermal noise.

Table 2

Performance comparison in hybrid architectures

Reference	Architecture	f_b kHz	ENOB	Power mW	FOM pJ
8	3rd-order LC-RC-SC	333	14.7	50	5.6
9	2nd-order 4-bit RC-SC	20	16.2	18	12.0
10	2nd-order 4-bit RC-SC	20	15.5	37	39.9
This work	2nd-order 5-bit RC-SC	500	13.5	5.8	1.0

The floor plan of the circuit depicted in Fig. 12 highlights the reduced size of the internal quantizer and the increased dimensions of the sampling capacitors. The digital part, comprising the two DEM encoders, the auto-ranging algorithm and the offset compensation for ten comparators, is relatively small with respect the total area of 600 μm ×900 μm. Tab. 3 provides a detailed summary of the each block.

These results demonstrate that hybrid architectures have the potential to combine the benefits of both continuous and discrete time implementations. The multi-bit technique is essential as a mean of reducing the power consumption of both the modulator and the PLL, not included in FOM estimations. Adaptive quantization, digital offset compensation in the quantizer, full clock-cycle sampling and encoder segmentation further allows reducing the power dissipation.

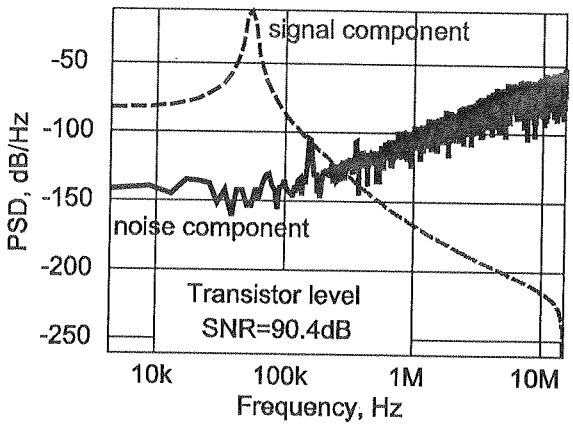

Fig. 11. Transistor-level simulated power spectral density

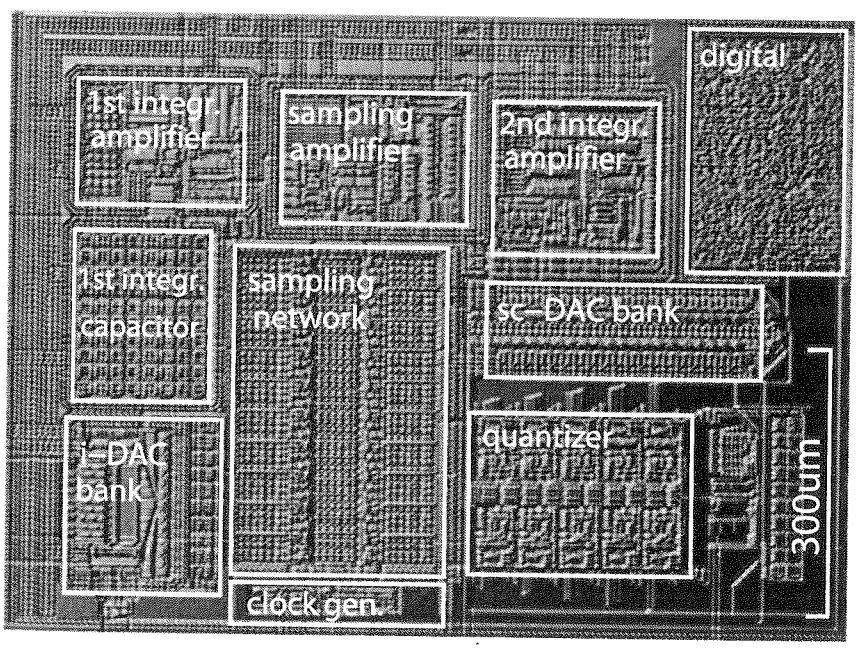

Fig. 12. Floor plan of the circuit in a CMOS 0.18 um technology

Table 3

Consumption and chip area summary

Component	Current μA	Area mm^2
CT integrator amp.	205	0.03
SC integrator amp.	1150	0.04
Sampling amp.	425	0.04
i-DAC	100	0.04
SC-DAC	140	0.04
ADC comparators	545	0.05
Digital circuits	500	0.04
Interconnect and 10 pF	–	0.07
Sampling capacitors	–	0.10
Total	3200	0.54

7. REFERENCES

1. X. Lu: *A novel signal-predicting multi-bit Delta-Sigma modulator.* Proc. of the IEEE International Conference on Electronics Circuits and Systems, December 2004, pp. 105-108.
2. C. Zierhofer: *Adaptive Sigma-Delta modulation with one-bit quantization.* IEEE Trans. on circuits and systems, May 2000, pp. 408-415.
3. L. Dorrer, and al.: *A 3-mW74-dB SNR 2-MHz continuous-time Delta-Sigma ADC with a tracking ADC quantizer in 0.13-um CMOS.* IEEE J. of Solid-State Circuits, vol. 37, December 2002, pp. 1636-1644.
4. S. Pesenti, P. Clement, M. Kayal: *Reducing the number of comparators in multi-bit Delta-Sigma modulators*, IEEE Transactions on Circuits and Systems II, accepted for publication.
5. A. Fishov, E. Siracusa, J. Welz, E. Fogleman, I. Galton: *Segmented mismatch-shaping D/A conversion.* Proc. Of the IEEE International Symposium on Circuits and Systems, vol. 4, May 2002, pp. 679-682.
6. S. Yan, S. Sanchez: *A continuous-time Sigma-Delta modulator with 88-dB dynamic range and 1.1-MHz signal bandwidth.* IEEE J. of Solid-State Circuits, vol. 39, January 2004, pp. 75-86.
7. M. Kappes: *A 2.2-mW CMOS band-pass continuous-time multi-bit Delta-Sigma ADC with 68 dB of dynamic range and 1 MHz bandwidth for wireless applications.* IEEE J. of Solid-State Circuits, vol. 38, July 2003, pp. 1098-1104.
8. R. Schreier, J. Lloyd, L. Singer, D. Paterson, M. Timko, M. Hensley, G. Patterson, K. Behel, J. Zhou: *A 10-300-MHz IF-digitizing IC with 90-105-dB dynamic range and 15-33-kHz bandwidth.* IEEE J. of Solid-State Circuits, vol. 38, December 2003, pp. 1098-1104.
9. K. Nguyen, R. Adams, K. Sweetland, H. Chen: *A 106-dB SNR hybrid Over-sampling analog-to-digital converter for digital audio.* IEEE J. of Solid-State Circuits, vol. 40, December 2005, pp. 2408-2414.
10. P. Morrow, M. Chamarro, C. Lyden, P. Ventura, A. Abo, A. Matamura, M. Keane, R. O'Brien, P. Minogue, J. Mansson, N. McGuinness, M. McGranaghan, I. Ryan: *A 0.18 um 102 dB-SNR mixed CT SC audio-band Delta-Sigma ADC.* IEEE International Solid-State Circuit Conference, 2005, pp. 178-179.

11. S. Haykin, B. van Veen: *Signals and Systems.* John Wiley & Sons Inc., New-York, 1999.
12. S. Pesenti: *Hybrid continuous-discrete-time multi-bit Delta-Sigma A/D converters with auto-ranging algorithm.* PhD dissertation, EPFL, Lausanne, accepted by the jury, to be published in 2008.
13. M. Pastre, M. Kayal: *Methodology for the digital calibration of analog circuits and systems with case studies.* Springer, Berlin, 2006.
14. M. Kayal, M. Pastre: *Automatic Calibration of Hall Sensor Microsystems.* Microelectronics Journal.
15. M. Pastre, M. Kayal, H. Blanchard: *Continuously gain-calibrated Hall sensor analog front-end for current measurement.* International Solid-State Circuits Conference (ISSCC), February 6 to 10-San Francisco-USA.

ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY, 2007, 53, no 4, pp. 379–388

Investigation of substrate noise coupling and isolation characteristics for a 0.35 μm HV CMOS technology

WALTER C. PFLANZL, EHRENFRIED SEEBACHER

Walter C. Pflanzl, Ehrenfried Seebacher are with austriamicrosystems AG, Schloss Premstaetten, A-8141 Unterpremstaetten, AUSTRIA.
e-mail: walter.pflanzl@austriamicrosystems.com

Received 2007.09.12
Authorized 2007.11.07

This paper presents the characterization of substrate noise coupling and the isolation capability of ohmic substrate contacts in a HV CMOS technology. Layout variations of contact sizes, distances, and several p+ guard structures are subject of this research. Metal shielded DUT fixtures have been developed to improve the reliability and accuracy of the measurements. All test cases are fabricated with a 0.35 μm HV CMOS technology (Vmax <= 120V). This process features high resistive native substrate (20 Ohm.cm) together with a 0.5 Ohm.cm pwell. The modeling section describes the distributed substrate "resistor" and the DUT fixture behavior.

Keywords: substrate coupling, isolation, guard ring, HV CMOS

1. INTRODUCTION

Substrate coupling becomes more and more a hot topic for modern process technologies [1] [2]. Especially in the case of mixed signal designs, it is absolutely essential to estimate the possible interactions between digital and analog blocks in order to avoid crosstalk [3]. The classical interaction generated by digital switching noise is challenging to suppress to analoge circuits and often RF frontends are limited by these interferences. Today excellent TCAD software is available but for such design issues not accurate enough. Substrate effects are mainly determined by parasitics which are the reason why simulations are not sufficient enough thus a testchip is a must.

The use of a multi die system is usually the best solution, but nevertheless, single die solutions are more cost effective and thus highly preferred.

2. SUBSTRATE COUPLING – OVERVIEW

Coupling paths. Substrate coupling is a very complex topic because there are many possible coupling scenarios: Devices like CMOS/HBTs [4], resistors, capacitors and interconnect structures inject additional currents into the substrate through inductive and/or capacitive coupling.

Substrate coupling can also be regarded as a lack of isolation capability. To describe such isolation effects the emphasis is put on special damping structures like guard rings.

Substrate. This paper basically investigates a very simple structure: Ohmic substrate contacts. The novelty in this case is the investigation of a 0.35 µm high voltage CMOS process, capable to handle with Vmax <= 120V. This process is based on p-type substrate with 20 Ohm.cm and a 0.5 Ohm.cm pwell.

3. TEST CHIP DESIGN AND TEST SCENARIOS

In order to get a detailed picture of substrate coupling diverse structures have been fabricated (Fig. 1). The test scenarios include distance and area variations of substrate contacts (Fig. 2), p+ guard ring isolation structures with diverse contact spacings (GRS), and ring thicknesses (GRT) (Fig. 3) [5]. Additionally structures with a metal shield beneath the signal pad to avoid coupling to substrate are also subject of interest (Fig. 2).

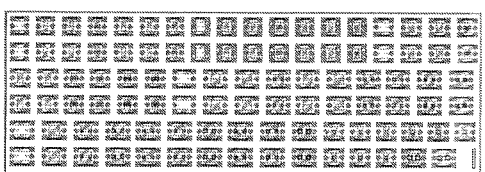

Fig. 1. The whole testchip at a glance

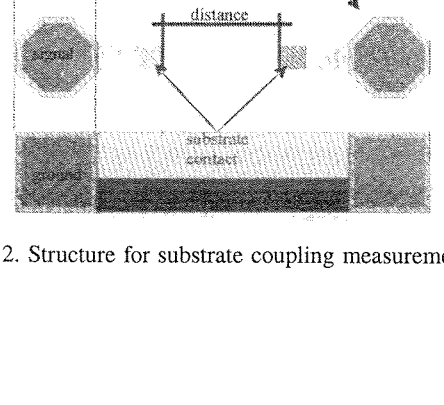

Fig. 2. Structure for substrate coupling measurement

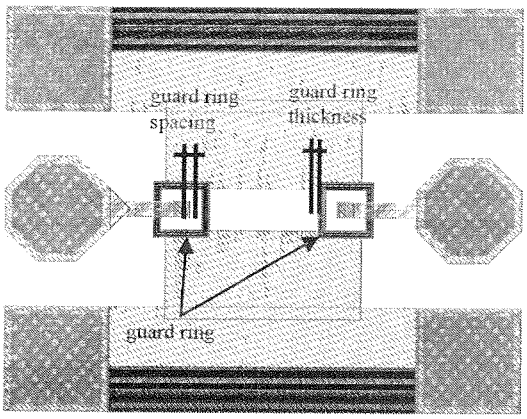

Fig. 3. Structure with p+ guard ring isolation

4. MEASUREMENT SETUP

DC Measurement. The parallel and series resistances of the test structures have been checked with a high precision multimeter. The obtained values are in accordance with s-parameter measurements and were used as the main input for modeling.

RF Measurement. The noise coupling between "aggressor" and "victim" was characterized with s-parameter measurements of the transfer parameter |S12| or |S21| (in case of symmetrical structures both are of same magnitude). This was done with an AGILENT^{tm} 8722D VNA from 0.1 to 40 GHz with Inifinity^{tm} GSG probes (100μm pitch) on a manual Cascade^{tm} probestation.

Measurement accuracy. DC measurements are basically most accurate and easy to realize whereas RF measurements are critical. Especially the dynamic range of the receiver in the VNA is the limiting part. In case of on wafer measurements additionally probe crosstalk lowers the dynamic response dramatically, which is also a function of distance of the probes.

5. CHARACTERIZATION RESULTS

Ohmic substrate contact. The first investigated structure includes ohmic substrate contacts in pwell at distances varied from 25, 50, 100 and 200 μm (Fig. 4) [6]. It can be observed that in first order damping increases linear with distance but there is also a trend observable, especially at 100 to 200 micron distance, that damping increases much more. This effect is discussed later under the topic "additional effects".

Fig. 5 shows the measurements for a similar test case like in Fig. 4 but includes now p+ guard rings. The contact area was A = 10×10 μm, guard ring spacing (GRS) 10 μm

and the guard ring thickness contains three contact rows (GRT = 3). A clear trend of distance variation can be seen. The most effective measure to obtain good damping is the introduction of the guard ring. An increased distance between "agressor" and "victim" as remedy for isolation is by far not as effective [7].

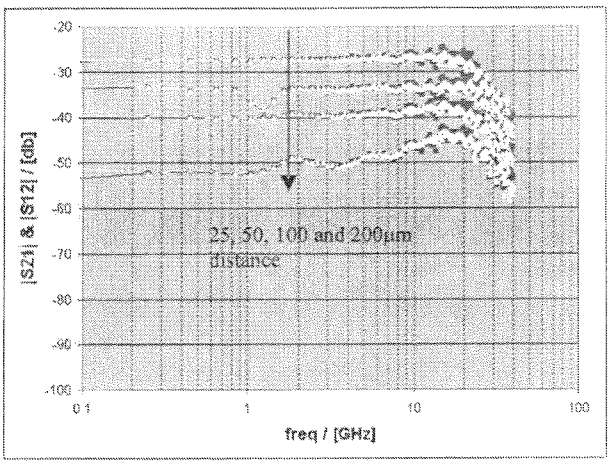

Fig. 4. Damping of pwell substrate contacts (area = 10×10 µm)

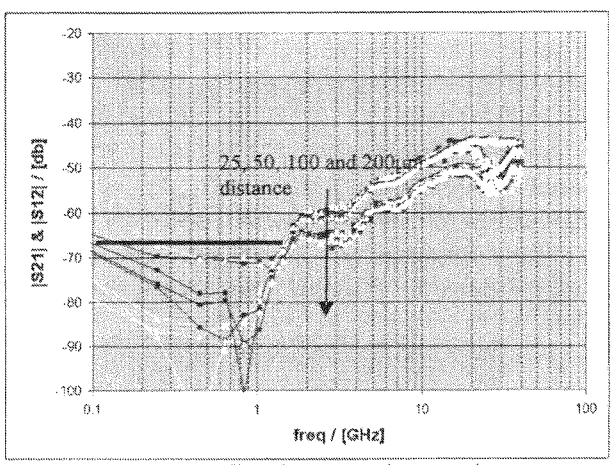

Fig. 5. Damping of pwell with p+ guard ring isolation at "victim" and "aggressor" side.
(A = 10×10 µm, GRT = 3, GRS = 10 µm)

Layout variations of p+ guard rings. Several layout variations have been investigated with following values: Contact area with 10×10 µm and with 20×20 µm, guard ring spacing varied from 2.5, 5 and 10 µm and the guard ring were designed with three, six and twelve parallel contact rows.

The results can be seen as an example in Fig. 6 and Fig.7, which are quite similar to Fig. 5. A tendency of some dB damping improvement can be seen only in the range <= 1 GHz for better guard ring to substrate connections with doubling the contact rows (Fig. 7) and a placement of the guard ring as close as possible to the "aggressor" and to the "victim" (quarter the GRS) (Fig. 6).

A small summary valid for freq. <= 1 GHz can be seen in the table below for A = 10×10 μm and for a substrate contact distance of 25 μm:

Fig. 4: No guard ring → –27 dB
Fig. 5: GRT = 3, GRS = 10 mm → –68 db
Fig. 6: GRT = 3, GRS = 2.5 mm → –73 dB
Fig. 7: GRT = 12, GRS = 2.5 mm → –75 db

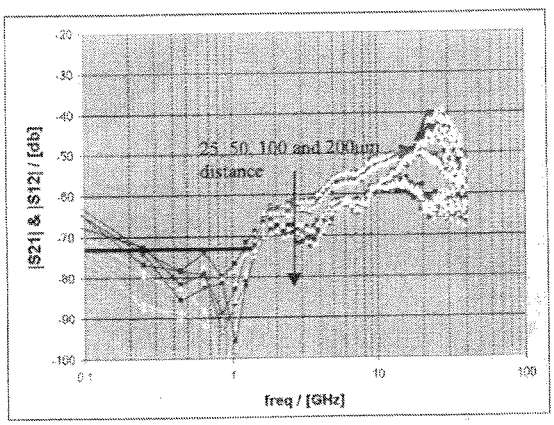

Fig. 6. Damping of pwell with p+ guard ring isolation (A = 110×10 μm, GRT = 3, GRS = 2.5 μm)

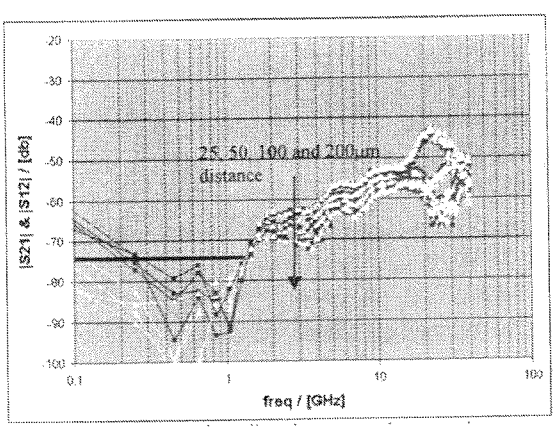

Fig. 7. Damping of pwell with p+ guard ring isolation (A = 10×10 μm, GRT = 12, GRS = 2.5 μm)

Metal shielded DUT structures. To guarantee reliable measurements the influence of the pad to substrate coupling had to be checked.

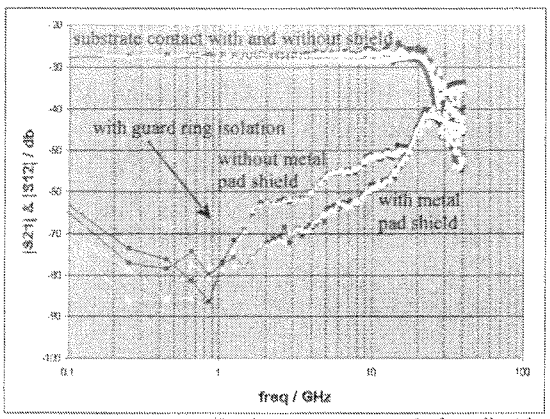

Fig. 8. Damping of pwell substrate contact and of pwell with p+ guard ring isolation – with and without metal pad shield

In the case of substrate pwell connections there is no difference recognizable (Fig. 8), but in the case of high isolation guard ring structures one can observe an improvement of up to 10 dB. This can be explained in the following way: The pad to substrate capacitance is negligible in the case of a pwell connection without guard rings whereas in the case of additional guard rings this capacitance becomes an important part. Thus metal shielded pads are essential to improve the s-parameter measurements for substrate coupling.

6. MODELING SECTION

Ohmic substrate contact. In this section the modeling of a substrate contact without any isolation structure (contact area = 10×10 μm, contact distance = 25 μm) is presented (Fig. 9) [8] [9] [10].

The SPICE simulation (Fig. 10) is in good agreement with the measurement (Fig. 11). The modeling takes over the resistancs from the DC measurements and the additional inductive and capacitive values are fitted with a MATLAB^{tm} routine [11].

The core of the schematic consists of a Π-resistor network which reflects the distributed "substrate resistor"; additional the parasitics are taken into account by inductances and by the pad to substrate capacitors [12].

p+ guard ring. The resistance values are again from the DC measurements and the inductances and capacitance values are calculated for best fit. The SPICE schematic (Fig. 12) can reproduce the measurement (Fig. 14) in quite good agreement (Fig. 13).

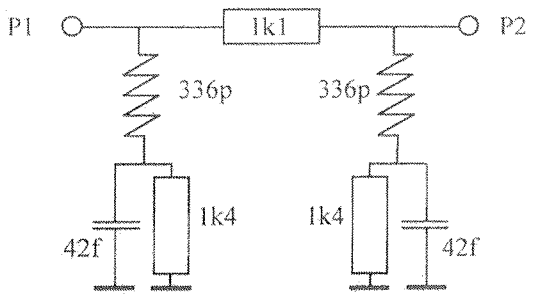

Fig. 9. Schematic for pwell substrate contact test structure. The resistances are taken over from DC measurments, the remainder device data are fitted values

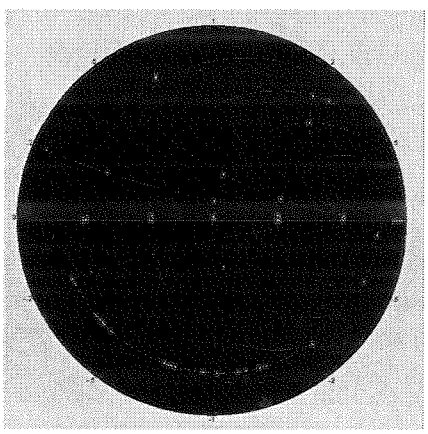

Fig. 10. Simulation of the schematic for a substrate connection (because of symmetry: |S11| = |S22| and |S21| = |S12|)

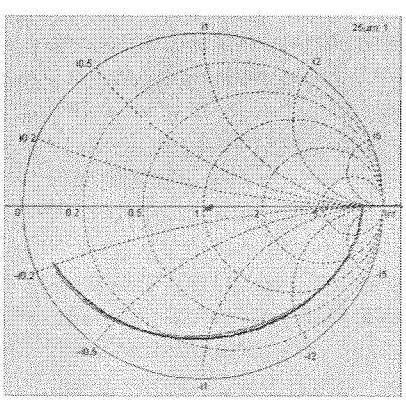

Fig. 11. Measurement data for comparison to Fig. 10

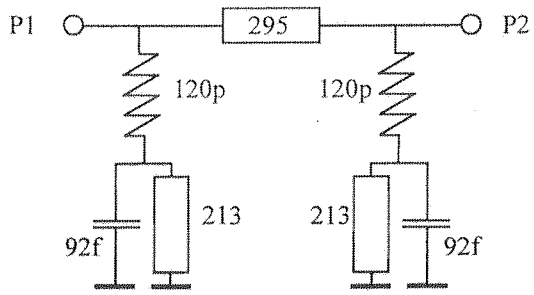

Fig. 12. Schematic for pwell substrate contact structure with p+ guard ring. Only the device values are changed

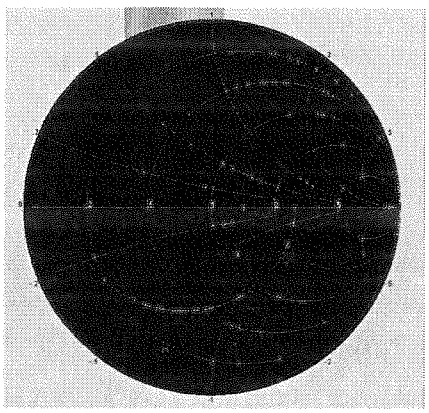

Fig. 13. Simulation of the schematic for an p+ isolated substrate connection

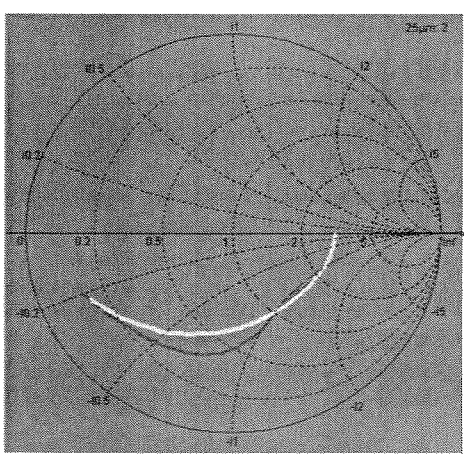

Fig. 14. Measurement data for comparison in case of a p+ isolated substrate contact

7. ADDITIONAL EFFECTS

"Guard ring effect of bare structure". Due to area saving no circle structures have been fabricated [13] in order to get as much test szenarios as possible on one chip. The disadvantage is that a kind of "guard ring effect" takes place which is shown in Fig. 15:

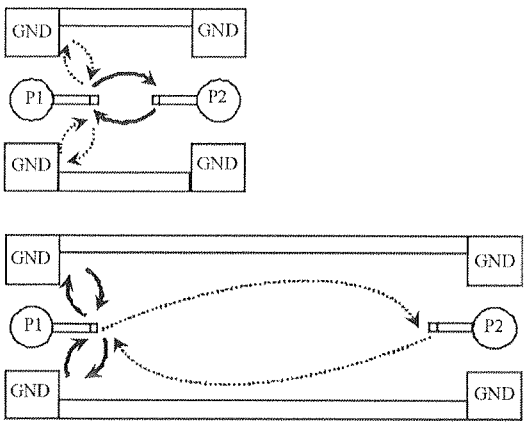

Fig. 15. Schematic for understanding the "guard ring effect" of bare structure due to grounding. The upper structure mainly couples via substrate. The longer the distance between the substrate contacts (bottom picture), more coupling takes place to the ground pads which is illustrated by thick arrows

Due to grounding the DUT structure, the interaction changes from the substrate contacts to the ground pads. This additional effect has to be taken into account interpreting the measurement data. The longer the distance in between the substrate contacts, the more of this effect can be observed.

8. CONCLUSIONS

Substrate coupling has been investigated for substrate contacts in a 0.35 μm HV CMOS process (Vmax <= 120 V, 20 Ohm.com substrate, 0.5 Ohm.cm pwell).

It is shown that p+ guard rings can provide a quite good damping behavior for frequencies <= 1 GHz. The isolation does not strongly depend on the layout. For reliable measurements additional metal pad shields are applied to suppress unwanted capacitive pad to substrate coupling.

All measurement results are checked for plausibility and measurement accuracy.

9. REFERENCES

1. X. Aragonès, et. al.: *Substrate Coupling Trends in Future CMOS Technologies*, Departament d'Enginyeria Electronica, Barcelona.
2. W. Steiner: *Reducing Substrate Coupling in 10 to 40 Gbit/s High-Gain Broadband Amplifiers*, Ruhr-University Bochum, Germany.
3. P. Basedau, Q. Huang: *A Post Processing Method for Reducing Substrate Coupling in Mixed-Signal Integrated Circuits*, Integrated Systems Laboratory, Swiss Federal Institute of Technology, Zurich, Switzerland.
4. M. Pfost: *An Experimental Study on Substrate Coupling in Bipolar/BiCMOS Technologies*, IEEE Journal of Solid-State Circuits, Vol. 39, No. 10, October 2004 s. 1755.
5. V. Liberali: *Reducing the Coupling to the Substrate in High-Speed Data Converters*, ESD-MSD Course on CMOS Data Converters for Communications Bellaterra, Barcelona (Spain) – May 10, 2002.
6. S. M. Sinaga, et al.: *Modeling and Analysis of Substrate Coupling in Silicon Integrated Circuits*, Delft University of Technology, ECTM/DIMES.
7. T. Blalack, et al.: *On-chip RF Isolation Techniques*, BCTM 21.1, Oct. 1, 2002.
8. F. Sischka: *Handling Silicon substrate effects in EM simulators*, presentation from AGILENT.
9. Ch. Xu, et al.: *High Frequency Lumped Element Models for Substrate Noise Coupling*, School of EECS, Oregon State University, Corvallis, OR 97331.
10. E. G. Friedman: *On-Chip Interconnect: The Past, Present, and Future*, 1st NoC Workshop – DATE '06 March 10, 2006.
11. W. Hoelzl: *Modellierung von MOS Transistoren für die SPICE²-Simulation von Analogen, Integrierten Schaltkreisen*, Master's Thesys, Techn. Univ. Graz, 1988.
12. G. Murata, K. Kundert: *A Substrate Modeling Methodology*, www.designers-guide.org
13. R. M. Vinella, et al.: *Substrate Noise Isolation Experiments in a 0.18 μm 1P6M Triple-well CMOS Process on a Lightly Doped Substrate*", IMTC 07.

Electronic Package Characterisation Using Thermal Structure Functions

JEDRZEJ BANASZCZYK[1], MARCIN JANICKI[2], BJORN VERMEERSCH[1], GILBERT DE MEY[1], ANDRZEJ NAPIERALSKI[2]

[1]*Department of Electronics and Information Systems, University of Ghent, Sint Pietersnieuwstraat 41, 9000 Ghent, Belgium*
[2]*Department of Microelectronics and Computer Science, Technical University of Lodz, Al. Politechniki 11, 90-924 Lodz, Poland*

Received 2007.09.20
Authorized 2007.11.13

This paper presents an overview of advanced thermal analysis methods. The measured heating or cooling curves allow the derivation of time constant spectra, structure functions and complex thermal impedances. These characteristics contain a lot of information on the device, and can be used to investigate the internal structure of the electronic package. The entire methodology is illustrated based on the example of two silicon carbide power diodes. These diodes provided by different manufacturers have the same ratings and package type but one of the diodes exhibits oscillatory behaviour when used in a power converter. The presented results of thermal tests and analyses confirmed that there exist between the two devices important differences in their internal structures, possibly indicating the presence of some imperfections in the die attach or the wire bonds.

Keywords: Thermal structure functions, electronic package properties, network identification by deconvolution, thermal impedance

1. INTRODUCTION

Recent intensive research in the thermal management of electronic systems has led to the development of new dynamic thermal analysis methods and tools. Some of these tools turned out to be useful not only for the solution of purely thermal problems but also found their application in the identification of structure geometry or material physical properties, fault detection, etc. In particular, this paper will demonstrate how to apply these methods for the investigation of electronic device packages. First an overview of the thermal measurement and analysis methods, together with some of

their underlying theory, is given. In the second part of the paper the example of two SiC power diodes is used to illustrate how the proposed methods are able to indicate internal package faults.

2. THERMAL ANALYSIS THEORY

Before different types of thermal analyses of a given structure can be carried out it is necessary to perform adequate temperature measurements. Therefore, initially this section will discuss some important issues related to electronic circuit temperature measurements. Then, various thermal analysis tools and methods, such as the structure functions and the thermal impedances will be explained in detail.

2.1. THERMAL TRANSIENT MEASUREMENT

The temperature measurements of an electronic circuit can be taken using a forward biased p-n junction. When the bias current is constant; the voltage drop across the junction serves as the measure of temperature. From the theoretical point of view temperature should be measured as a response to the power step excitation. However, this solution requires using the same junction both for heating and measurement, which might cause some technical problems during the practical realisation. An alternative approach, used also in this paper, is to heat the junction till steady state condition is reached and to switch the power off. In this way a cooling curve is captured. Providing that, as explained later, some basic requirements are met, and assuming that a given system is linear, the cooling curve is the compliment of the heating curve and contains exactly the same information.

The key issue in the measurements of thermal transient responses is the time resolution of the recorded data. Namely, measured structures usually consist of multiple layers made of different materials (silicon chip, package, cooling assemblies), each having different geometry and thermal properties. Consequently, the thermal response curves are a superposition of many exponential curves corresponding to different time-constants, which might span even over 6 decades in time. Therefore, equidistant sampling on the logarithmic time scale should be used for the acquisition of thermal transient curves. Only then all the time-constants can be identified.

Similarly, since the thermal transients are very rapid, the most important temperature changes happen in the very beginning. Thus, the logarithmic time scale is advisable also when presenting graphically results of transient thermal measurements.

2.2. NETWORK IDENTIFICATION BY DECONVOLUTION

The thermal time-constants can be identified from the measurements employing the Network Identification by Deconvolution (NID) method, which was originally de-

veloped in the eighties by Szekely and van Bien [1]. This method uses thermal transient data equally spaced on the logarithmic time scale as it was explained before. Next, a deconvolution operation is carried out and the time-constant spectrum is computed. Then, the spectrum can be further transformed into the structure functions, which are introduced in the following subsection.

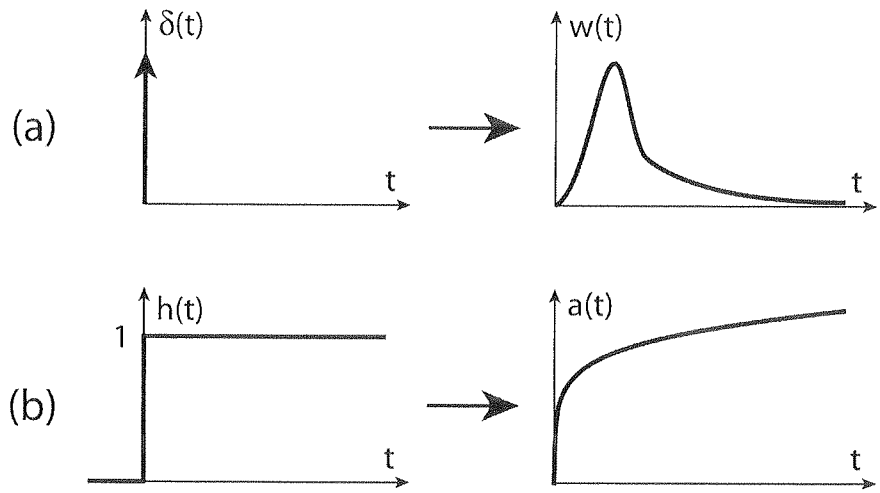

Fig. 1. Dirac-delta (a) and unit-step (b) functions with their respective responses

From the network theory it is known that time responses of a linear circuit to arbitrary excitations can be found as the convolution of a particular excitation and some characteristic functions $w(t)$ and $a(t)$, which are circuit responses to the Dirac-delta function $\delta(t)$ and the unit-step function $h(t)$ respectively (see Figure 1). For the feasibility reasons, the unit-step function $h(t)$ is usually used in practice. Conversely, if the temperature response to a given excitation is known, it is possible to determine the corresponding characteristic functions performing a deconvolution.

Each real structure can be subdivided into smaller parts transferring heat to the neighbouring regions. If power is applied to a single point of the structure, it is possible to construct an equivalent one-dimensional model which produces exactly the same temperature response. Such a model takes the form of an equivalent RC network. Thus, each network can be fully characterized with the time-constant spectrum, by specifying the exact position and the magnitude of its time-constants. Because real physical structures are continuous their time-constant spectra are also continuous and become spectral density functions. For such distributed systems, their thermal responses to the unit step excitations can be found from the time-constant spectra using the following formula:

$$a(t) = \int_0^\infty R_{th}(\tau)\,[1 - exp(-t/\tau)]d\tau \tag{1}$$

When the time variables t and τ in the above equation are replaced with their logarithmic counterparts z and ξ and $exp(z - exp(z))$ is represented as $w_z(z)$, the following convolution integral can be derived [2]:

$$\frac{d}{dz}a(z) = \int_0^\infty R_{th}(\xi) \cdot w_z(z - \xi)\, d\xi \tag{2}$$

Consequently, for an exemplary time-constant spectrum shown in Figure 2, three dominant time-constants can easily be identified at τ_1, τ_2, τ_3.

Concluding, according to the NID method, the time-constant spectrum can be found by subsequent execution of the following tasks: the acquisition of the heating/cooling curve, the derivation of the recorded curve and the numerical deconvolution.

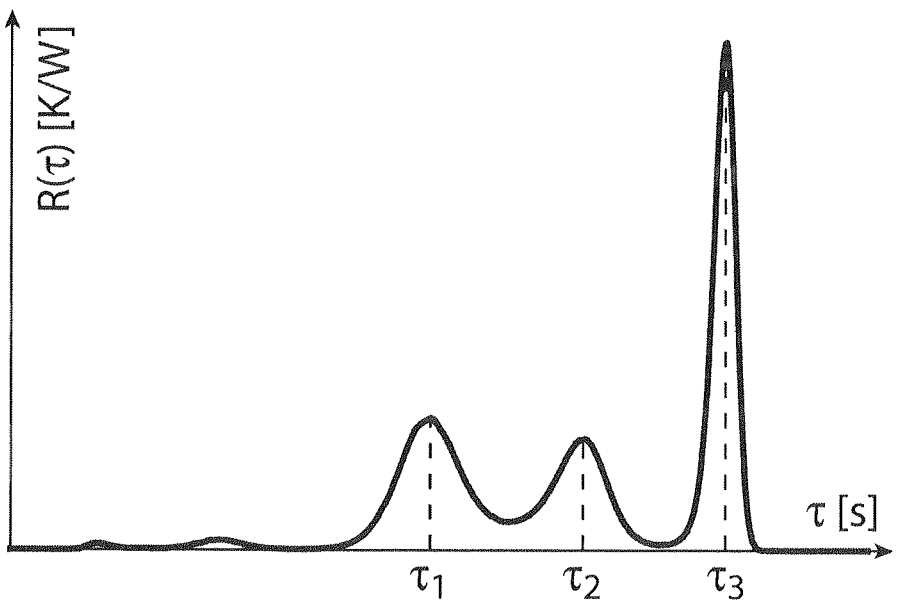

Fig. 2. Exemplary time-constant spectrum

2.3. STRUCTURE FUNCTIONS

The computed time-constant-spectra can be used to obtain the so-called structure functions which are extremely useful for the thermal analysis of electronic circuits. With finite accuracy, continuous spectra can be discretized to obtain the Foster canonical form representation, which in turn can be converted to the Cauer canonical form [3].

The Cauer networks can be represented, as illustrated in Fig. 3, by the so-called cumulative structure functions $C_\Sigma(R_\Sigma)$, which constitute a kind of thermal resistance

and capacitance map for the entire heat-flow path. The origin corresponds to area where the power is dissipated, while the singularity at the end can be associated to the ambient. The plateaus in the curve relate to a certain mass of material from where the C_{th} values can be read.

The derivative of the cumulative thermal capacitance with respect to the thermal resistance is the differential structure function. This function, also shown in Figure 3, is extremely useful as well. The peaks, which are easily visible, correspond to the changes in material through which heat is diffusing, so they can be attributed to different stages of the heat flow path, such as the chip, the package or the cooling assembly.

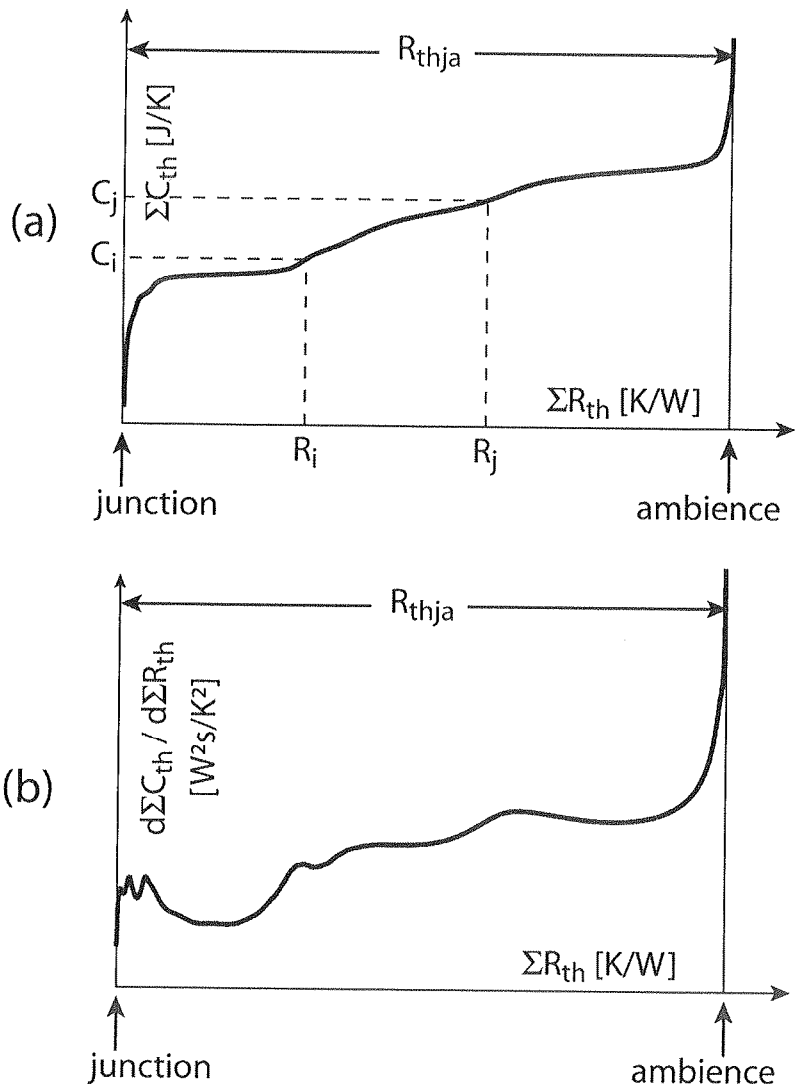

Fig. 3. Exemplary cumulative (a) and differential (b) structure functions

Because the differential capacitance K is proportional to the square of the cross-sectional area of the heat-flow path, it is possible to determine the dimensions of the particular layers in an examined structure. The structure functions allow the reconstruction of the structure or the heat-flow path, with the resolution of about 20 points along the path. They render possible the identification of the partial thermal resistances, as well as the detection and the localization of the heat-transfer irregularities. Therefore, structure functions are excellent tools for the thermal characterisation of electronic structures and the detection of their faults.

2.4. THERMAL IMPEDANCE

Another possible way to describe the dynamic thermal behaviour of electronic circuits is to utilize the complex thermal impedance. This impedance can be computed performing the Laplace transform of the measured structure transient thermal response.

The manufacturers of electronic circuits usually provide in their data sheets the junction-to-ambient thermal resistance. This value contains information only about the steady state operation of the circuit. The information about the dynamic thermal behavior is conveyed by the thermal impedance curve. The thermal impedance Z_{th} is defined as the ratio between the temperature rise and the dissipated power. When power is continuously supplied to the circuit the temperature increases until the system reaches steady state. Then the thermal impedance and resistance are equal. The thermal impedance as a function of frequency can be represented in the complex plane by the Nyquist plot with the angular frequency as the parameter, as shown in Figure 4.

The thermal impedance plot is a very convenient tool, which characterizes the thermal behaviour of the entire system including the silicon chip, the package and the cooling mount. The Nyquist plot shown in Figure 4 corresponds to the thermal time-constant spectrum presented in Figure 2. Each of the components in the transient response corresponding to a dominant time-constant will give rise to a circular arc in the Nyquist plot. The so called central frequency (i.e. observed in the point at the bottom of the circles), is closely related to the reciprocal of the corresponding time-constant τ. Note however that if the dominant time-constants are lying relatively close to each other, the circles can no longer be distinguished separately. Some of the arcs will merge together, leading to a curve as shown in Figure 4. More detailed theory about the thermal impedance and its properties can be found in [4]-[6].

3. PRACTICAL EXAMPLE

To illustrate the capabilities of the NID method in practice, two silicon carbide Schottky diodes were investigated. These devices, both in TO-220 packages and rated for the same current and voltage, were made by different manufacturers from the same semiconductor substrates. Thus, theoretically they should behave similarly. However,

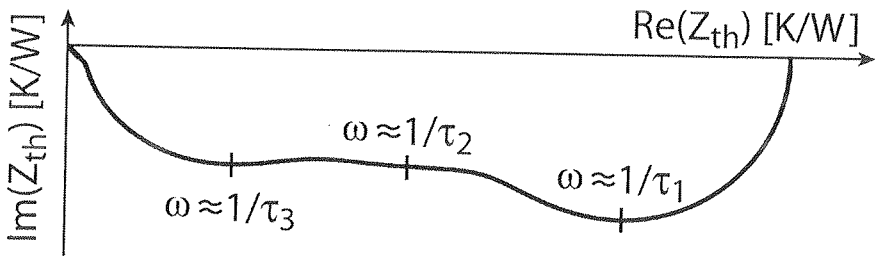

Fig. 4. Exemplary Nyquist plot of thermal impedance

when used in a power converter, unexpected oscillatory behaviour during the switch-off of one of the diodes was observed. Such a result might be caused by a poor connection or partial delamination inside the package, e.g. at the leads, as this introduces some parasitic elements in the electrical circuit. To investigate this problem, the earlier described thermal analyses were performed, providing us information about the internal package structure.

For the investigation we used the thermal transient tester T3Ster manufactured by the Micred company, a part of the Flomerics group. The tester is capable of applying a power step to the diode and sampling its junction temperature with the very high time resolution of 1 μs. The result of the measurement is a temperature cooling or heating curve. Based on the measured curves, the software, provided also by the Micred company together with the thermal tester, allows the robust extraction of the time-constant spectrum and the thermal impedances by means of the NID method. A diode is a one-port device with one p-n junction which at the same time plays the role of a heat source and a temperature sensor. Due to this fact it is impossible to dissipate heat and measure the temperature of the junction simultaneously. That is why in our measurements we had to resort to the cooling curves. As mentioned before, when using cooling curves we assume that the system is linear. Furthermore, we need to be sure that at the end of the heat-up phase the system has reached equilibrium before the measurement is started, otherwise a special correction algorithm has to be used [7].

In order to increase the resolution, the measurements were taken in the conditions assuring small thermal impedance to ambient. Namely, the devices were attached to a large heat sink and placed in a wind tunnel. The wind speed was set to the maximum attainable in this tunnel, i.e. 4.15 m/s. Owing to this set-up, it was possible to emphasize the heat flow path inside the package and gain information on the internal package structure. The forward diode current was equal to 2 A, as in the original power converter. This caused the temperature rise of almost 13 K for the power of 2.76 W.

The measured cooling curves, containing the information on the heat flow path between the junction and the ambient, were processed further in order to obtain the thermal time-constant distribution, the thermal impedance plot and the corresponding differential structure function presented in Figures 5-7 respectively.

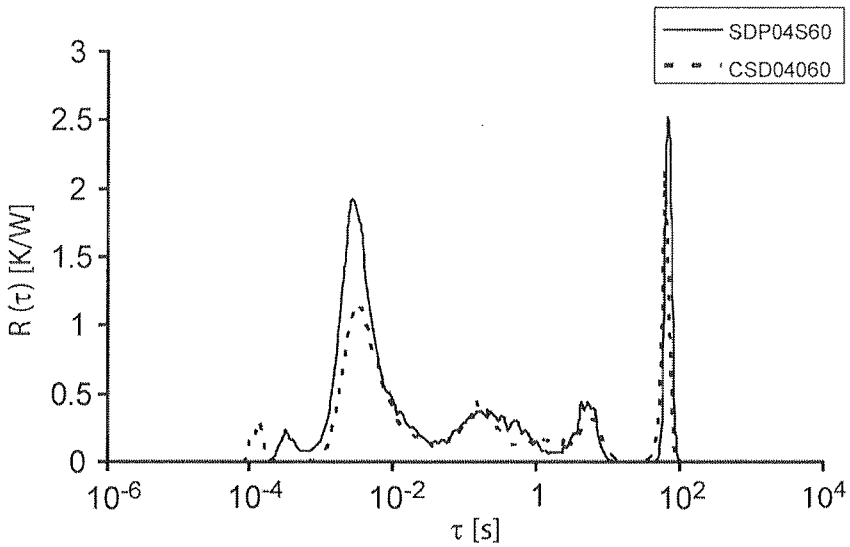

Fig. 5. Time-constant spectrum of the investigated diodes

The obtained time-constant distribution clearly shows that there are five peaks located between the values of 100 μs and 100s. These peaks correspond to the particular sections of the heat flow path, i.e. the chip, the package and the radiator. As can be seen, the replacement of the diode affects only the two peaks related to the most inner parts of the package. The first time-constant is shifted by some 200 μs to the right for the SPD04S60 diode.

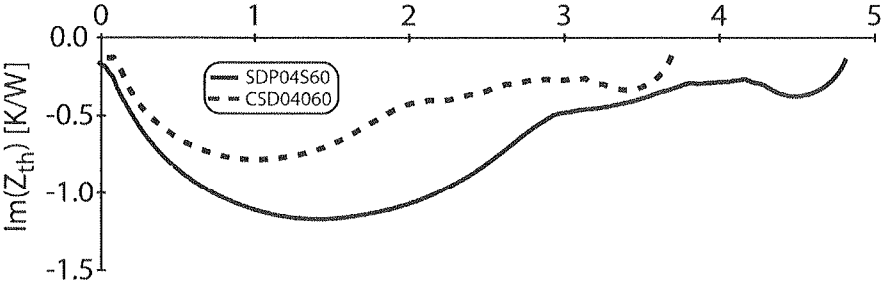

Fig. 6. Thermal impedance plots of the measured diodes

What is more, for the same diode the second time-constant corresponding to a few milliseconds is considerably bigger, which confirms the presence of an additional thermal impedance inside the package. This might indicate that there exist some wire bond or die attach of high thermal and electrical resistivity. Otherwise the thermal time-constant spectra are almost identical, signifying that the only differences are in

the internal structure close to the semiconductor die and that the outer packages have the same thermal properties.

By comparing the thermal impedance plots we make similar observations. The leftmost circle, corresponding to the internal part of the package, is much bigger for the SPD04S60, while the low frequency parts of the plots have the same shape in both cases. Again, this suggests a presence of an additional thermal impedance inside the package. It is difficult to recognize circles in the portion of the plot related to the package. If we take a look at the time-constant spectrum we will see that the time-constants for the middle-frequencies are rather distributed than sharply defined. This gives rise to many circles with similar centre frequencies, which merge and result in a rather irregular curve. However, if the time-constants are sufficiently separated in time the circles can be easily observed, as in the case of the leftmost and rightmost ones, corresponding to the chip and the heat sink respectively.

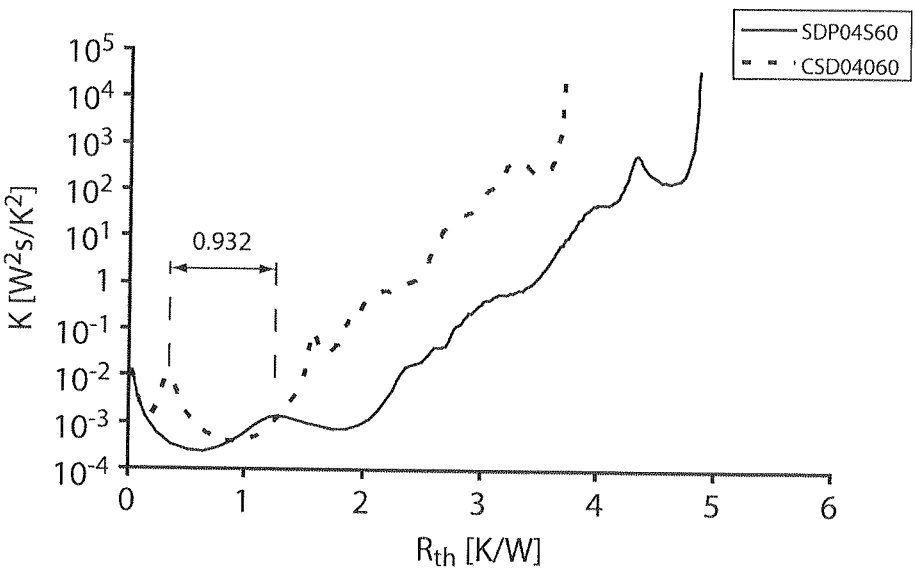

Fig. 7. Differential structure function

The analysis of the differential structure functions of the Schottky diodes leads to similar conclusions. The peaks in these structure functions indicate consecutive layers of material in the package. The first peak visible in both curves represents the silicon substrate and the last one is the package body. Finally, the curves tend to infinity, which represents the infinite thermal capacitance i.e. the surrounding ambient. As can be seen, in the case of the SDP04S60 diode the second peak is considerably flattened and shifted. This indicates a presence of an extra thermal impedance of almost 1 K/W, presumably air voids in the die attach, caused by a faulty contact between the leads and the substrate.

4. CONCLUSIONS

The presented results of the research confirm that the NID method and other related dynamic thermal analysis tools might prove extremely useful in the investigation of the internal structure of electronic packages and the identification of package faults or other imperfections. Similar results to the ones presented here were published in [8], where the authors used the same equipment for the investigation of a power transistor in the TO-220 package.

5. ACKNOWLEDGEMENTS

This research has been supported by the grant of the Polish Ministry of Science and Higher Education No. N515 008 31/0331.

Bjorn Vermeersch is working as a Research Assistant for the Research Foundation – Flanders (FWO – Vlaanderen) and wishes to thank FWO for supporting the presented work.

6. REFERENCES

1. V. Szekely, T. Van Bien: *Fine structure of heat flow path in semiconductor devices: measurement and identification method.* Solid-State Electronics 1998, vol. 31, pp. 1363-1368.
2. V. Szekely: *On representation of infinite-length distributed RC one-ports.* IEEE Trans. on Circuits and Systems 1991, vol. 38, pp. 711-719.
3. M. Rencz, V. Szekely, A. Poppe, G. Farkas, B. Courtois: *New methods and supporting tools for the thermal transient testing of packages.* Intl. Conference on Advances in Packaging APACK (Singapore). Dec. 2001, pp 407-411.
4. P. Kawka: *Thermal impedance measurements and dynamic modelling of electronic packages.* PhD Thesis, Universiteit Gent, Ghent, Belgium, 2005.
5. J. Banaszczyk: *Thermal impedance measurements of electronic packages.* MSc Thesis, Politechnika Łódzka, Łódź, Poland, 2006.
6. B. Vermeersch, G. De Mey: *Thermal impedance plot of microscaled devices.* Microelectronics Reliability 2006, vol. 46, pp. 174-177.
7. F.N. Masana: *Correction to thermal impedance measurements under non-equilibrium conditions.* XIV Int. Conference on Mixed Design of Integrated Circuits and Systems MIXDES (Poland). Jun. 2007, pp 369-374.
8. P. Szabo, O. Steffens, M. Lenz, G. Farkas: *Transient junction-to-case thermal resistance: measurement methodology of high accuracy and high repeatability.* IEEE Trans. Components and Packaging Technologies 2005, vol. 28, no. 4, pp. 630-636.

ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY, 2007, 53, no 4, pp. 399–406

Adaptive High Side Power Switch for automotive applications

P. DEL CROCE, J. HADZI-VUKOVIC, B. MELDT, M. LADURNER

Infineon Austria, Siemensstrasse 2, 9500 Villach, Austria
E-mail: Paolo.DelCroce@infineon.com
Telephone: +43 5 1777 6232
Fax: +43 5 1777 6698

Received 2007.09.27
Authorized 2007.11.15

This paper presents a design approach based on the splitting of the power transistor for smart power applications. The design approach is applied to realize a High Side Power Switch with a configurable output in Smart Power Technology. Experimental results are also presented and discussed.

Keywords: Smart Power, High Side Power Switch, DMOS

1. INTRODUCTION

Protections and diagnosis became more and more important in automotive power applications. Main reason for this trend are safety requirements, high reliability and complex power management of modules in a car. Within the last few years the number of power modules in the automotive environment has rapidly increased. Smart power high side drivers are not simple switches any more, but also systems for providing information about power and fault conditions. The high side power switch has to withstand fault conditions like short circuit, reverse battery, inverse current operation or overvoltage. The on-resistance of switches is typically in the range of 6 to 200 mΩ. Most of the applications require PWM operation with frequencies between 50 and 200 Hz typically to serve the needs of loads like bulbs, small motors or heating systems.

Vertical Power MOSFETs have been attracting a lot of attention in last few decades. They are used for a variety of low voltage power switching applications because of their superior forward conduction characteristics, high switching speed, high input impedance, good thermal stability and easy integration [1]. High current, high power

MOSFETs are integrated monolithically with a planar IC technology which allows the design of controls, interfaces and protective circuits. The outcome is a technology class known as "Smart Power" [2, 3]. Choosing both the processing technology and the design methodology carefully, high performance with high fabrication yield and low costs can be obtained [4]. This makes a large chip surface area more economically viable, and the power dissipation for different current values can be optimized by sizing the Power MOSFET (DMOS) area [5]. A trade off between optimum static losses and DMOS area is still necessary due to chip cost constrains. By minimizing transition times (rise and fall time) the energy dissipation during switching (which is significant for loads driven with Pulse Width Modulation, PWM) can be reduced. A trade off is also necessary between dynamic losses and switching time, due to Electro-Magnetic Interference (EMI) [6]. EMI can be reduced using different techniques, but design effort and area requirement for reliable results are quite demanding [7]. Due to the different application trade offs, designing versatile and cost effective products is a challenging task. In this paper we report a flexible solution for a High Side Power Switch realized in smart power technology and we discuss the results of its implementation. An analog approach can also be applied to Low Side Power Switches.

2. ADAPTIVE POWER SWITCH

A modern power switch is able to be much more than a simple relay. It is controlled via digital inputs and can be equipped with a Serial Peripheral Interface (SPI) for use in microcontroller-based applications. It performs load switching with a controlled output slope (Slew Rate, SR) and timing (Turn ON/OFF Time, T_{ON}/T_{OFF}) for controlling switching losses and EMI. It has embedded protection features against output short circuit (current limitation, I_{LIM}) and overtemperature (thermal shutdown) conditions for improved reliability. It provides feedback on load current (a sensing current $I_{SENSE} = I_{LOAD} / K$ is provided at the Sense Pin IS), open load and overload for enhanced diagnostic strategies [8]. In the steady state condition, the switch is characterized with an On State Resistance (R_{ON}). A block level description of a modern high side power switch is shown in Fig. 1.

According to the load type and application, the suitably configured switch should be selected. However, from the manufacturing and assembling point of view, it would be cheaper to use the same switch type for different loads. In cars, the problem often faced is where LED lightning is mixed with fluorescent bulb lightning; an example of such an application is presented in Fig. 2. Here for LED and bulb back lights a different power switch would be required, otherwise not all the loads can be driven in the most efficient way. For this reason an adaptive power switch can be a cost-effective solution when being used with such mixed load boards.

The switching module is equipped with a single versatile component and the most suitable configuration is defined via software from the application itself. Each configuration requires specific switching parameters, according to the following considerations:

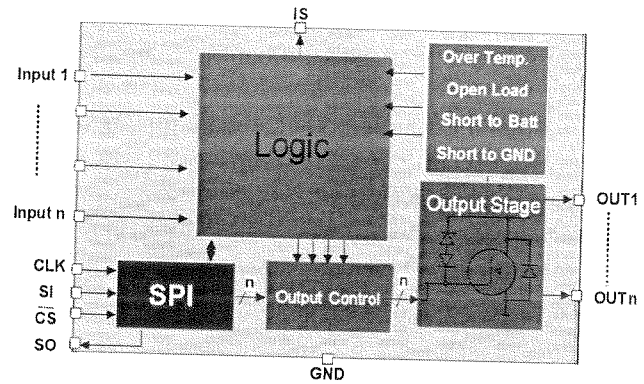

Fig. 1. Block level description of a modern High Side Power Switch

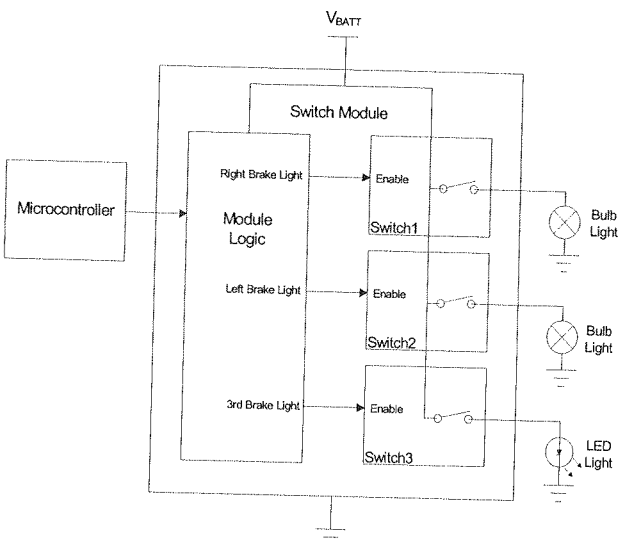

Fig. 2. Example of switching module for mixed lightning application

- Slew-Rate and switching time (SR, T_{ON}/T_{OFF})
  LED lights are mainly driven with PWM and the duty-cycle can vary in the full range 1-99% for dimming, so high slew-rate and short switching times are required. The fast switching does not have any drawback in terms of EMI due to the reduced current consumption. For bulbs this is not the case, so the slew rate must be reduced and the switching time consequently increased.
- Current Limit (I_{LIM})
  To ensure proper switching of bulb lamps (current of cold bulb lamp is approximately ten times the nominal value in the first milliseconds) and adequate protection of thin LED wiring, the current limit must be adjusted according to the target load.

- Load to Sense current ratio (K)
  For the different nominal load currents, the constant "K" in the formula $I_{SENSE} = I_{LOAD}/K$ must be adjusted. For an accurate diagnostic it is necessary to get, in both cases, an I_{SENSE} in the range of hundreds of microamperes for the nominal output current.
- Power MOS On State Resistance (R_{ON})
  It is a key parameter in case of bulb lamps and is directly related to power losses (not so important in the case of LED).

3. DESIGN APPROACH

Design target in this paper is a High Side Power Switch capable of two different output configurations named "Bulb" and "LED". The configuration "Bulb" is optimized for driving bulb lamps and the configuration "LED" is optimized for driving LED lights. Differences between the two configurations are described in Table 1. The set of parameters in "LED" mode are obtained scaling the values in "Bulb" mode by a common factor N. Making use of the constant ratio N, it is possible to get the desired results with the output configuration in Fig. 3, where N = 3 has been chosen. A Power DMOS is used for switching, while a small part of the same device (Sense DMOS) is used for output current sensing. The DMOS is driven with a constant gate current ($I_{CHARGE}/I_{DISCHARGE}$) and the switch T1 is programmed according to the selected "LED" or "Bulb" mode. An Operational Amplifier (OA) ensures the same biasing at the Power and the Sense DMOS for better sensing accuracy. All the circuitry (charging/discharging block, current sensing block and current limitation block) are designed according to the specifications in "Bulb" mode with the switch T1 closed. Opening T1, the DMOS active area decreases to 1/3 of the original size and the gate capacitance scales accordingly. In agreement to the gate charging equation (1), a reduction in gate capacitance results in a faster switching:

$$\frac{\partial V_{GATE}}{\partial t} = \frac{I_{GATE}}{C_{GATE}} \tag{1}$$

Opening T1 increases the slew rate by a factor of three and the switching time decreases by the same factor. Because the Sense and Power DMOS have the same drain-source voltage, the load to sense current ratio can be written as:

$$K = \frac{I_{LOAD}}{I_{SENSE}} = \frac{PowerDMOS_{Area}}{SenseDMOS_{Area}} \tag{2}$$

From equation (2), with T1 being open, the load to sense current ratio is three times smaller. Since the current limitation circuit refers to I_{SENSE}, the output current limit decreases by a factor three as well. The specifications for "LED" mode are obtained simply by opening T1. No additional circuitry in the DMOS Driver stage is necessary

Table 1

Design requirement: differences between "LED" and "Bulb"

Parameter \ Mode	"Bulb"	"LED"
Slew-Rate$_{ON}$ = dV/dT$_{ON}$	SR_{ON}	SR_{ON} *N
Slew-Rate$_{OFF}$ = dV/dT$_{OFF}$	SR_{OFF}	SR_{OFF} *N
Turn ON time	T_{ON}	T_{ON}/N
Turn OFF time	T_{OFF}	T_{OFF}/N
Output current limitation	I_{LIM}	I_{LIM}/N
I_{SENSE}	I_{LOAD}/K	(I_{LOAD}/K)*N

apart for T1, so the impact in terms of area is quite low if compared with other solutions [9]. As a benefit for design robustness, no reconfigurations of the analog stages (i.e. gate charging, gate discharging, current monitor and current limitation blocks) are needed. Moreover, this approach brings a benefit in terms of current sensing accuracy based on the fact that the DMOS R_{ON} increases in "LED" mode (higher DMOS drain-source voltage reduces the impact of the operational amplifier offset on sensing accuracy).

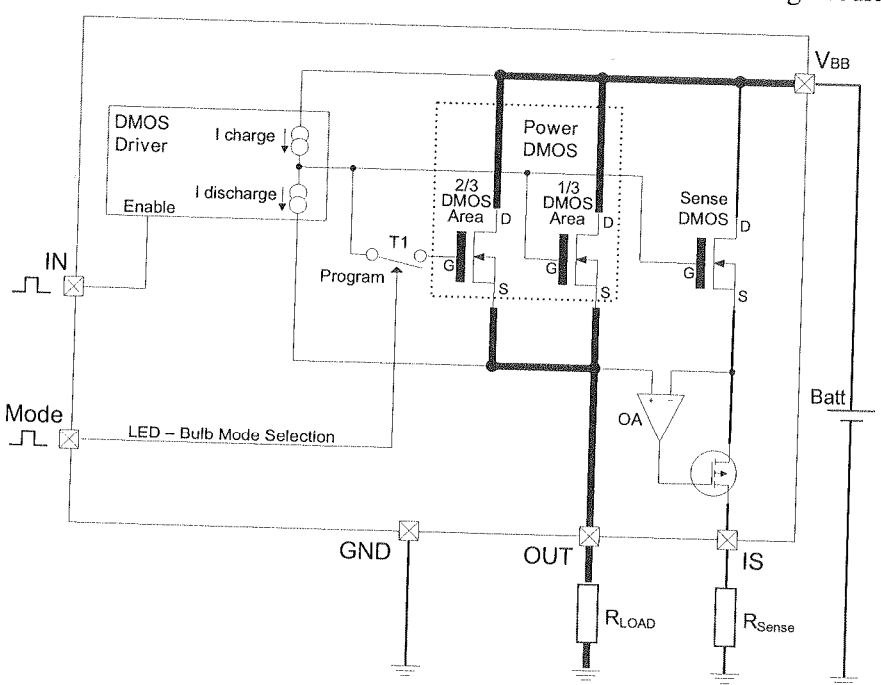

Fig. 3. Selection of switch configuration based on DMOS splitting

Mode selection, as shown in Fig. 3, is done via an external pin, but can be controlled via an internal SPI as well. In principle at each load switching a different

switching mode can be selected. Two configurations have been implemented, but with further partitioning of the DMOS and adding T_i switches, the number of modes M can increase according to the application. For the present realization the overall Power DMOS area has been defined to have a 20 mΩ ON resistance. Additional parameters for "Bulb" mode are: SR = 200 mV/µs, I_{LIM} = 22 A, K = 3000.

4. EXPERIMENTAL RESULTS

A lot of twenty samples has been packaged in a power plastic package and measured over a wide temperature range using automated test equipment for high volume production [10]. The results are presented in figures 4-6. The three figures present key parameters of all twenty samples as function of temperature. This way of presenting results is typical for automated test equipment. Figure 4 presents the output to sense current ratio "K". The parameter has been measured with a load current of 2A in "Bulb" mode and 0.5A in "LED" mode. "K" scales as expected (factor three) and due to the increased resistance in "LED" mode the sensing accuracy remains good in the low current range. Using the same loads, the switching performance has also been measured.

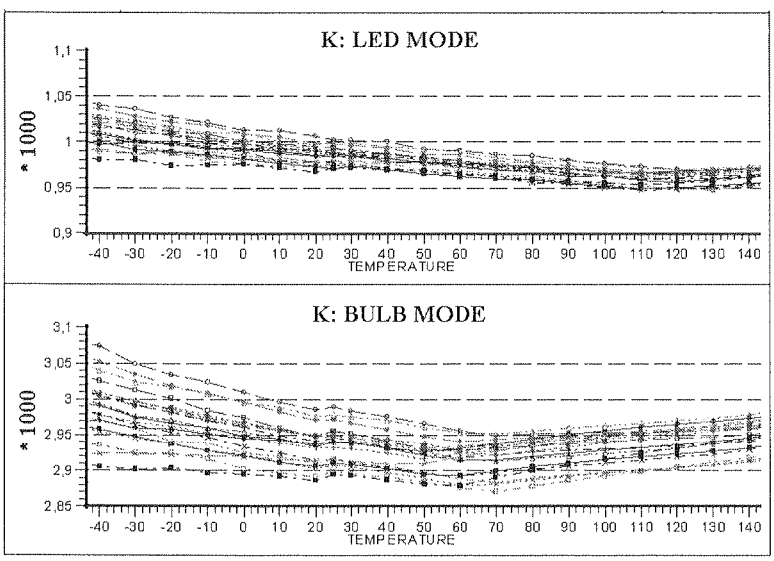

Fig. 4. "K" factor measured over temperature on 20 samples for both "LED" and "Bulb" loads

Results are presented in Figure 5 as the output slew rate. The parameter scales down from "LED" to "Bulb" mode by a factor about 2.7. Responsible for the shift from target value are capacitances connected to the DMOS gate line in the driver stage. Reducing them is possible to get closer to the target "LED / Bulb" ratio (three in this case). The curve bending visible in Bulb mode at high temperature for the most of the

samples is caused by a weakness of the DMOS driver and is not related to the splitting concept. Figure 6 presents values of the current limitations measured under short circuit condition with a battery voltage of 13.5V. The short circuit measurement set-up is the same for both "LED" and "Bulb" mode. The current limit scales as expected.

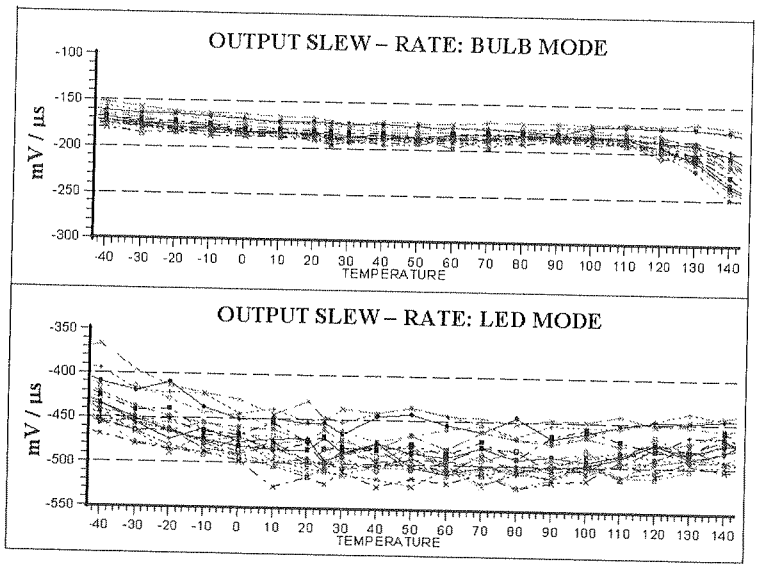

Fig. 5. Slew-rate measured over temperature on 20 samples for both "LED" and "Bulb" loads

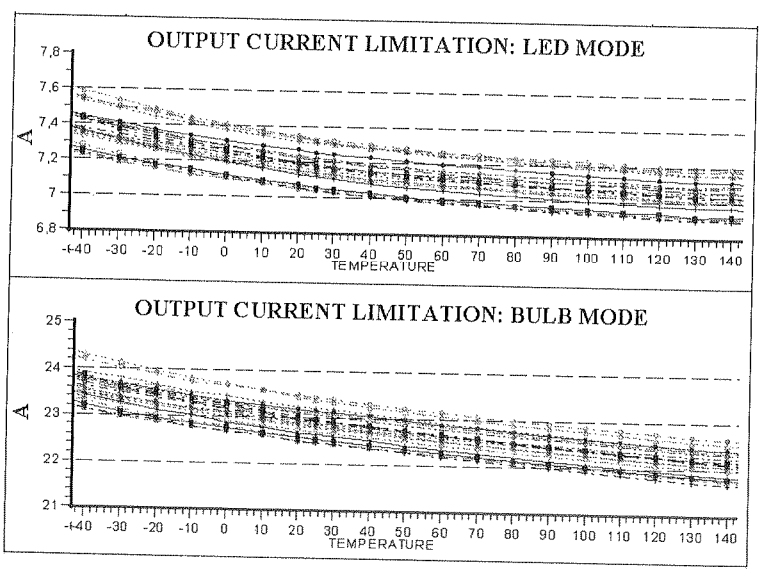

Fig. 6. Output current limit measured over temperature on 20 samples for both "LED" and "Bulb" loads

5. CONCLUSION

A design method for the realization of adaptive power switches has been introduced. M is defined as the number of potential output configurations of a single switch or application modes. M is theoretically not limited. The configuration can be selected at any time via a dedicated pin or, if available, SPI command. An implementation of a high side power switch in Smart Power Technology with M = 2 optimized for driving LED and bulb lamps has been presented. The measurement results confirm the expectations, but also suggest a more accurate evaluation of the overall capacitance at the DMOS gate line is needed. DMOS splitting technique appears as a promising solution in terms of performance, design effort, cost and product reliability for the realization of adaptive power switches and a variety of smart power circuits which contain large power transistors.

6. REFERENCES

1. C. W. Richard, D. W. Tsang, K. P. Lisiak: *A high performance planar power MOSFET*, IEEE Trans. on Electron devices, Vol. 27, pp. 340-343, 1980.
2. R. S. Wrathall, D. Tam: *Integrated circuits for the control of high power*, Proceedings of IEEE International Eelectron Device Meeting IEDM, pp. 408-411, 1983.
3. J. Einzinger, L. Leipold, J. Tihanyi, R. Weber: *Monolithic IC power switch automotive applications*, Proceedings of IEEE International Solid State Circuits Conference, pp. 22-23, 1985.
4. A. Elmoznine, J. Buxo, M. Bafluer, P. Rossel: *The smart power high-side switch: description of a specific technology, its basic devices, and monitoring circuitries*, IEEE Trans. on Electron devices, Vol. 37, pp. 1154-1161, 1990.
5. R. P. Love, P. V. Gray, M. S. Adler: *A large-area power MOSFET designed for low conduction losses*, IEEE Trans. on Electron devices, Vol. 31, pp. 817-820, 1984.
6. R. Monteiro, B. Borges, V. Anunciada: *EMI reduction by optimizing the output voltage rise time and fall time in high-frequency soft-switching converters*, Proceedings of IEEE Power Electronics Specialists Conference, pp. 1127-1132, 2004.
7. S. Musumeci, A. Raciti, A. Testa, A. Galluzzo, M. Melito: *Switching-behavior improvement of insulated gate-controlled devices*, IEEE Trans. on Power electronics , Vol. 12, pp. 645-653, 1997.
8. A. Graf: *Smart power switches for automobile and industrial applications*, proceedings of VDE ETG Conference "Contact performance and switching", pp. 1-8, 2001.
9. "D388A Electroluminenscent lamp and white LED driver IC", Data Sheet, Rogers Corporation, http://www.rogerscorporation.com/
10. I. A. Grout: *Integrated Circuit Test Engineering* Springer, London 2006.

INFORMATION FOR AUTHORS OF E.T.Q.

An article published in other magazines can not be submitted for publishing in E.T.Q. TThe size of an article can not exceed 30 pages, 1800 character each, including figures and tables.

Basic requirements

The article should be submitted to the editorial stuff as a one side, clear, black and white computer printout in two copies. The article should be prepared in English. Floppy disc with an electronic version of the article should be enclosed. Preferred wordprocessors: WORD 6 or 8.

Layout of the article.

- Title.
- Author (first name and surname of author/authors).
- Workplace (institution, adress and e-mail).
- Concise summary in a language article is prepared in (with keywords).
- Main text with following layout:
  - Introduction
  - Theory (if applicable)
  - Numerical results (if applicable)
  - Paragraph 1
  - Paragraph 2
  - .....
  - .....
  - Conclusions
  - Acknowledgements (if applicable)
  - References
- Summary in additional language:
  - Author (firs name initials and surname)
  - Title (in Polish, if article was prepared in English)
  - Extensive summary, hawever not exceeching 3600 characters (along with keywords) in Polish, if artide was prepared in English). The summary should be prepared in a way allowing a reader to obtaoin essential information contained in the artide. For that reason in the summary author can place numbers of essential formulas, figures and tables from the article.

Pages should have continues numbering.

Main text

Main text cannot contain formatting such as spacing, underlining, words written in capital letters (except words that are commonly written in capital letters). Author can mark suggested formatting with pencil on the margin of the article using commonly accepted adjusting marks.

Text should be written with double line spacing with 35 mro left and right margin. Titles and subtitles should be written with small letters. Titles and subtitles should be numberd using no mor than 3 levels (i.e. 4.1.1.).

Tables

Tables with their titles should be places on separate page at the end of the article. Titles of rows and columns should be written in small letters with double line spacing. Annotations concerning tables should be placed directly below the table. Tables should be numbered with Arabic numbers on the top of each table. Table can contain algorithm and program listings. In such cases original layout of the table will be preserved. Table should be cited in the text.

Mathematical formulas

Characters, numbers, letters and spacing of the formula should be adequate to layout of main text. Indexes should be properly lowered or raised above the basic line and clearly written. Special characters such as lines, arrows, dots

should be placed exactly over symbols which they ar attributed to. Formulas should be numbered with Arabic numbers place in brackets on the right side of the page. Units of measure, letter and graphic symbols should be printed according to requirements of IEE (International Electronical Commission) and ISO (International Organisation of Standardisation).

References

References should be placed at the and of the main text with th subtitle „References". Refrences should be numbered (without brackets) adequately to references placed in the text. Examples of periodical [@], non-periodical [2] and book [3] references:

1. F. Valdoni: A new milimetre wave satelite. E.T.T. 1990, vol. 2, no 5, pp. 141–148
2. K. Anderson: A resource allocation framework. XVI International Symposium (Sweden). May 1991. paper A 2.4
3. Y.P. Tvidis: Operation and modeling of the MOS transistors. Nw York. McGraw-Hill. 1987. p. 553

Figures

Figures should be clearly drawn on plain or milimetre paper in the format not smaller than 9 × 12 cm. Figures can be also printed (preferred editor – CorelDRAW). Photos or diapositives will be accepted in black and whit format not gratd than 10 × 15 cm. On th margin of each drawing and on th back side of each ohoto authorp name and abbreviation of the title of article should be placed. Figure's captures should be given in two languages (first in the language the article is writtes in and then in additional language). Figure's captures should be also listed on separate page. Figures should be cited in the text.

Additional information

On the separate page following information should be placed:

- mailing address (home or office),
- phone (home or/and office),
- e-mail.

Author is entiled to free of charge 20 copies of article. Additional copies or the whole magazine can be ordered at publisher at th one's expense.

Author is obliged to perform the author's correction, which should be accomplished within 3 days starting from the date of receiving the text from the editorial stuff. Corrected text should be returned to the editorial stuff personally or by mail. Correction marks should be placed on th margin of copies received from the editorial stuff or if needed on separate pages. In the case when the correction is not returned within said time limit, correction will be performed by technical editorial stuff of the publisher.

In case of changing of workplace or home address Authors are asked to inform the editorial stuff.

POLISH ACADEMY OF SCIENCE
COMMITTEE FOR ELECTRONICS AND TELECOMMUNICATIONS

ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY

KWARTALNIK ELEKTRONIKI I TELEKOMUNIKACJI

CONTENTS OF VOLUME 53/2007

WARSZAWA 2007

CONTENTS

Nr 1

Nr 2

Nr 3

Nr 4

THE LIST OF THE REVIWERS
ELECTRONICS AND TELECOMMUNICATIONS QUARTERLY

Dr inż. ***Adam Abramowicz***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Dr inż. ***Jarosław Arabas***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Jerzy Baranowski***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Dr inż. ***Andrzej Bąk***
Politechnika Warszawska,
Instytut Telekomunikacji

Dr hab. inż. ***Zbigniew Bielecki***
Wojskowa Akademia Techniczna
Warszawa

Dr inż. ***Piotr Bora***
Wojskowa Akademia Techniczna
Warszawa

Dr inż. ***Michał Borecki***
Politechnika Warszawaska
Instytut Mikro i Optoelektroniki

Dr inż. ***Tomasz Buczkowski***
Politechnika Warszawska
Instytut Radioelektroniki

Dr hab. inż. ***Bohdan Butkiewicz***
Politechnika Warszawska
Instytut Systermów Elektronicznych

Dr hab. inż. ***Grzegorz Ciesielski***
Politechnika Łódzka
Instytut Elektrotechniki Teoretycznej,
Metrologii i Materiałoznawstwa

Dr hab. inż. ***Witold Czarnecki***
Politechnika Warszawska,
Instytut Telekomunikacji

Dr inż. ***Krzysztof Czerwiński***
Politechnika Warszawska
Instytut Radioelektroniki

Prof. nzw. dr hab. ***Andrzej Dąbrowski***
Politechnika Warszawska
Instytut Telekomunikacji

Dr inż. ***Henryk Dobrowolski***
Politechnika Warszawska
Instytut Informatyki

Prof. dr hab. inż. ***Janusz A. Dobrowolski***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Dr inż. ***Jarosław Domaszewicz***
Politechnika Warszawska,
Instytut Telekomunikacji

Dr inż. ***Przemysław Dymarski***
Politechnika Warszawska,
Instytut Telekomunikacji

Prof. dr hab. inż. ***Jerzy Frączek***
Politechnika Śląska
Instytut Automatyki

Dr hab. inż. ***Piotr Gajewski***
Wojskowa Akademia Techniczna
Instytut Telekomunikacji, Warszawa

Dr inż. ***Piotr Gajowniczek***
Politechnika Warszawska
Instytut Telekomunikacji

Dr inż. ***Zbigniew Gajo***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Bogdan Galwas***
Politechnika Warszawska,
Instytut Mikroelektroniki
i Optoelektroniki

Dr inż. ***Sławomir Kula***
Politechnika Warszawska
Instytut Telekomunikacji

Prof. nadzw. dr hab. ***Zbigniew Kulka***
Politechnika Warszawska
Instytut Radioelektroniki

Dr inż. ***Krzysztof Kulpa***
Politechnika Warszawska
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Zygmunt Kuśmierek***
Politechnika Łódzka
Instytut Elektroniki Teoretycznej,
Metrologii i Materiałoznawstwa

Dr hab. inż. ***Wiesław Kuźmicz***
Politechnika Warszawska
Instytut Mikroelektroniki i Optoelektroniki

Prof. dr hab. inż. ***Juliusz Lech Kulikowski***
Polska Akademia Nauk, Warszawa
Instytut Biocybernetyki i Inżynierii Biomedycznej

Prof. dr hab. inż. ***Zygmunt Kuśmierek***
Politechnika Łódzka, Instytut Elektrotechniki
Teoretycznej, Meteorologii i Materiałoznawstwa

Dr inż. ***Lech Lewandowski***
Politechnika Warszawska
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Tadeusz Łuba***
Politechnika Warszawska,
Instytut Telekomunikacji

Dr inż. ***Janusz Marzec***
Politechnika Warszawska
Instytut Mikroelektroniki i Optoelektroniki

Mgr inż. ***Grzegorz Mazur***
Politechnika Warszawska,
Instytut Informatyki

Prof. dr hab. inż. ***Marian Miłek***
Politechnika Zielonogórska,
Instytut Metrologii Elektrycznej

Prof. dr hab. inż. ***Józef Modelski***
Politechnika Warszawska
Instytut Radioelektroniki

Prof. dr hab. inż. ***Tadeusz Morawski***
Politechnika Warszawska,
Instytutu Radioelektroniki

Prof. dr hab. inż. ***Jan Mulawka***
Politechnika Warszawska
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Andrzej Napieralski***
Politechnika Łódzka,
Instytutu Elektroniki

Prof. dr hab. inż. ***Andrzej Olszyna***
Politechnika Warszawska
Wydział Inżynierii Materiałowej

Dr inż. ***Leszek Opalski***
Politechnika Warszawska
Instytut Systemów Elektronicznych

Dr inż. ***Andrzej Pacut***
Politechnika Warszawska
Instytut Automatyki

Prof. dr ***Wincenty Pajewski***
Polska Akademia Nauk
Instytut Podstawowych Problemów Techniki

Dr hab. inż. ***Zdzisław Papir***
Akademia Górniczo-Hutnicza, Kraków
Katedra Telekomunikacji

Dr inż. ***Andrzej Paszkiewicz***
Politechnika Warszawska,
Instytut Telekomunikacji

Dr inż. ***Krzysztof Perlicki***
Politechnika Warszawska
Instytut Telekomunikacji

Dr inż. ***Halina Tarasiuk***
Politechnika Warszawska
Instytut Telekomunikacji

Dr hab. inż. ***Jan Petykiewicz***
Politechnika Warszawska,
Instytut Fizyki

Prof. dr hab. inż. ***Andrzej Pfitzner***
Politechnika Warszawska,
Instytut Mikroelektroniki
i Optoelektroniki

Prof. dr hab. inż. ***Stanisław J. Piestrach***
Politechnika Wrocławska
Instytut Cybernetyki Technicznej

Prof. dr hab. inż. ***Marian Piekarski***
Politechnika Wrocławska
Instytut Telekomunikacji i Akustyki

Prof. dr hab. inż. ***Anna Piotrowska***
Instytut Technologii Elektronicznej
Warszawa

Prof. dr hab. inż. ***Kazimierz J. Pluciński***
Wojskowa Akademia Techniczna
Instytut Podstaw Elektroniki, Warszawa

Dr inż. ***Sławomir Pluta***
Politechnika Opolska
Wydział Elektrotechniki, Automatyki
i Informatyki

Prof. dr hab. ***Włodzimierz Pogribny***
Akademia Techniczno-Rolnicza
Instytut Telekomunikacji, Bydgoszcz

Dr inż. ***Artur Przelaskowski***
Politechnika Warszawska
Instytut Radioelektroniki

Mgr inż. ***Mariusz Rawski***
Politechnika Warszawska
Instytut Telekomunikacji

Dr inż. ***Mirosław Rojewski***
Politechnika Gdańska,
Instytut Systemów Informacyjnych

Prof. nadzw. dr hab. ***Stanisław Rosłoniec***
Politechnika Warszawska
Instytut Radioelektroniki

Dr hab. ***Krzysztof Sacha***
Politechnika Warszawska
Instytut Automatyki i Informacji Stosowanej

Prof. dr hab. inż. ***Jerzy Siuzdak***
Politechnika Warszawska,
Instytut Telekomunikacji

Prof. nadzw. dr hab. ***Władysław Skarbek***
Politechnika Warszawska
Instytut Radioelektroniki

Dr inż. ***Andrzej Skorupski***
Politechnika Warszawska
Instytut Informatyki

Mgr inż. ***Krzysztof Skowroński***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Prof. zw. dr hab. ***Wojciech Sobczak***
Politechnika Gdańska
Katedra Systemów Informacyjnych

Prof. dr hab. inż. ***Waldemar Soluch***
Instytut Technologii Materiałów
Elektroniczych

Prof. dr hab. inż. ***Marek Stabrowski***
Politechnika Warszawska,
Instytut Elektrotechniki Teoretycznej
i Miernictwa Elektrycznego

Dr hab. inż. ***Witold J. Stepowicz***
Akademia Morska
Katedra Elektroniki Morskiej, Gdynia

Prof. dr hab. inż. ***Jerzy Szabatin***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Paweł Szczepański***
Politechnika Warszawska
Instytut Mikroelektroniki i Optoelektroniki

Dr inż. ***Feliks Szczot***
Politechnika Opolska
Wydział Elektrotechniki, Automatyki
i Informatyki

Dr hab. ***Jan Szmidt***
Politechnika Warszawska
Instytut Mikroelektroniki i Optoelektroniki

Prof. dr hab. inż. ***Mieczysław Szustakowski***
Wojskowa Akademia Nauk
Instytut Optoelektroniki, Warszawa

Dr inż. ***Jacek Szymanowski***
Politechnika Warszawska,
Instytut Automatyki i Informatyki Stosowanej

Dr inż. ***Lech Śliwa***
Politechnika Warszawska,
Instytut Podstaw Elektroniki

Dr inż. ***Marek Średniawa***
Politechnika Warszawska
Instytut Telekomunikacji

Prof. dr hab. inż. ***Leszek Trybus***
Politechnika Rzeszowska,
Katedra Automatyki i Informatyki

Prof. dr hab. inż. ***Aleksander Urbaś***
Politechnika Warszawska,
Instytut Systemów Eektronicznych

Prof. dr hab. inż. ***Krzysztof W. Wawryn***
Politechnika Koszalińska
Katedra Teorii Obwodów
i Układów Elektronicznych

Mgr inż. ***Krzysztof Włostowski***
Politechnika Warszawska
Instytut Telekomunikacji

Dr ***Piotr Witoński***
Politechnika Warszawska
Instytut Mikroelektroniki i Optoelektroniki

Płk. dr hab. inż. ***Marian Tadeusz Wnuk***
Wojskowa Akademia Techniczna
Instytut Telekomunikacji, Warszawa

Prof. dr hab. inż. ***Jacek Wojciechowski***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Prof. nzw. dr hab. inż. ***Andrzej Wojtkiewicz***
Politechnika Warszawska,
Instytut Systemów Elektronicznych

Dr. inż. ***Wojciech Wojtasiak***
Politechnika Warszawska
Instytut Radioelektroniki

Dr inż. ***Adam W. Woźniak***
Politechnika Warszawska
Instytut Automatyki

Prof. dr hab. inż. ***Waldemar Wójcik***
Politechnika Lubelska
Katedra Elektroniki

Prof. dr hab. inż. ***Józef Woźniak***
Politechnika Gdańska
Katedra Systemów Informacyjnych

Dr hab. inż. ***Zygmunt Wróbel***
Uniwersytet Śląski
Instytut Problemów Techniki

Dr inż. ***Wojciech Zabłotny***
Politechnika Warszawska
Instytut Systemów Elektronicznych

Prof. dr hab. inż. ***Janusz Zarębski***
Akademia Morska
Katedra Radioelektroniki Morskiej,
Gdynia