

# A New Design Methodology For Enhancing The Transient Loading Of Low Drop-out Regulators (LDRs)

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**Abstract**—A new simple design methodology which makes LDR output nearly insensitive to jumps of the load current for long times is proposed. This methodology is tested for more than  $10^4$  seconds. Our procedure leans on cross coupling of the time second derivative of the LDR power transistor gate and drain voltages along with their currents. This technique keeps low values of these currents in order of nano or hundreds of micro amperes for undershot or overshoot cases, respectively. The introduced methodology has been applied to a standard CMOS of  $0.18\mu\text{m}$  technology for NMOS transistors and validated using MATLAB R2014a.

**Keywords**—low drop-out regulator, cross coupling, jumps of the load current, undershot, overshoot

## I. INTRODUCTION

THE strategies of solving the transient load regulation problem for the LDR power transistor have different forms according to the approach of modeling of the transient current. In this regard, the actual transient terminal currents of MOS transistor must be described in terms of the normalized channel inversion charge density along the channel length. This is owing to the non-constant of the channel current along that length during the transient conditions. Amongst the approaches of solving the transient load regulation problem, there is one that considers only the spatial average of the transient channel and gate currents. All designs presented in [1-8] are based on such an approach. The procedure of these literatures depends on enlarging the regulator circuit slew rate. On the other hand, there is another approach that concerns with evaluating the effect of the spatial propagation component of the transient channel and gate currents. However, the normalized channel charge density used in determining these currents are modeled via the quasi static procedure. In that strategy, the normalized inversion charge density is computed by the static model formula which is a function only of the position along the channel and its value in transient state at the bounds [9]. Not all of the demonstrated approaches deal really

with the true mathematical description of the transient impact loading exerted on the LDR power transistor.

Our proposed methodology is based on modeling the solution of the continuity equation using symmetrical telescopic modification of the cubic sp-line collocation method [10] for the power transistor of the LDR. This methodology matches with the mathematical description of transient mode continuity equation and so it is expected to be more accurate and general. The generality doesn't mean establishing the methodology on specific modes of operations or limited scenarios as the case of slew rate improvement based algorithms [1-8]. Consequently, our new methodology is established on EKV compact MOS model. In addition, EKV model is a charge based model which facilitates applying our proposed technique on the sp-line collocation method. This paper is organized as follows. Section II demonstrates the derivation of the transient terminal currents. An overview on the cubic sp-line collocation method is described in section III. Section IV studies the effect of the application of the symmetrical telescopic modification of the cubic sp-line collocation method on the LDR power transistor. The explanation of the new proposed methodology is realized via section V. Section VI is concerned with displaying our simulation results and section VII summarizes our concluded remarks.

## II. TRANSIENT TERMINAL CURRENTS

The transient channel current is determined by continuity equation which has a mathematical form given by [11]:

$$\frac{\partial I(x,t)}{\partial x} = w \frac{\partial \rho_s(x,t)}{\partial t} \quad (1)$$

In the above formula,  $I(x, t)$  denotes the electron current along  $x$  direction of the channel at time  $t$ ,  $w$  is the channel width, and  $\rho_s(x, t)$  represents the surface inversion charge density. The channel current  $I(x, t)$  can be expressed as a function of the surface channel charge density  $\rho_s(x, t)$  as:

$$I(x,t) = -\mu w \frac{\partial \rho_s(x,t)}{\partial x} \left( \frac{\rho_s(x,t)}{N_\rho C_{ox}} - V_T \right) \quad (2)$$

In Eq.(2),  $\mu$  denotes the electron mobility,  $N_\rho$  represents the charge slope factor,  $C_{ox}$  symbolizes the oxide capacitance per unit area, and  $V_T$  indicates the thermal electro-dynamic voltage.

By substituting Eq.(2) into Eq.(1), the continuity partial differential equation in terms of  $\rho_s(x, t)$  can be formed. This continuity equation is general and can be fitted to any MOS device model. Owing to its charge based compact modality,

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EKV model is selected here. This selection facilitates the determination of boundary and initial conditions of the continuity equation. As a result, the normalized charge density and the mobility reduction effect will be introduced in terms of EKV model [12]. Thus, the surface inversion charge density can be formulated as:

$$\rho_s(x,t) = -\theta N_\rho C_{ox} V_T r_s(x,t) \quad (3)$$

with

$$\theta \triangleq \frac{1}{1+10C_{ox}} + \frac{1}{1+20C_{ox}} \quad (4)$$

and

$$\mu = \frac{\mu_0 K_1}{r_s(x,t) + K_2} \quad (5)$$

In the above mathematical expressions,  $\theta$  is a dimensionless factor which models the quantum non-idealities effects resulted from band gap widening and has an average value determined by Eq.(4),  $r_s(x, t)$  denotes the normalized inversion charge density,  $\mu_0$  symbolizes the low field mobility, and  $K_1$  &  $K_2$  are terminal voltage dependent parameters that model the effect of mobility reduction. The substitution of Eqs.(3-5) into Eq.(1) gives a new form for the continuity equation which becomes:

$$\frac{\partial r_s(x,t)}{\partial t} = \mu_0 \frac{K_1 V_T}{K_2} \left( \frac{\partial^2 r_s(x,t)}{\partial x^2} \left( 1 + \left( \theta - \frac{1}{K_2} \right) r_s(x,t) - \frac{\theta}{K_2} r_s^2(x,t) \right) + \left( \frac{\partial r_s(x,t)}{\partial x} \right)^2 \left( \theta - \frac{1}{K_2} - \frac{2\theta}{K_2} r_s(x,t) \right) \right) - \frac{1}{N_\rho} \frac{dN_\rho}{dt} r_s(x,t) \quad (6)$$

On the other hand, the boundary conditions are evaluated by the EKV model compact formula between the normalized channel charge density and the channel voltage. This is achieved by the solution of the following algebraic equations:

$$v(0,t) = \frac{1}{V_T} \left\{ \frac{V_G(t) - V_B(t) - V_{th}}{N_V} - [V_S(t) - V_B(t)] \right\} = \ln r_s(0,t) + 2r_s(0,t) \quad (7)$$

$$v(L,t) = \frac{1}{V_T} \left\{ \frac{V_G(t) - V_B(t) - V_{th}}{N_V} - [V_S(t) - V_B(t)] \right\} = \ln r_s(L,t) + 2r_s(L,t) \quad (8)$$

In the above formulas,  $v(0, t)$  represents the normalized overdrive voltage at the source, whilst  $v(L, t)$  denotes the same thing at the drain,  $V_G(t)$  is the gate voltage,  $V_B(t)$  is the bulk voltage,  $V_{th}$  is the threshold voltage which is a dependent parameter on the terminal voltages,  $V_S(t)$  is the source voltage,  $V_D(t)$  is the drain voltage,  $r_s(0, t)$  is the normalized inversion charge density at the source, and  $r_s(L, t)$  denotes the same thing at the drain. Furthermore, the initial conditions can be obtained through the assignment of the channel current at any position  $x$  to the initial average current for the whole length of the channel  $L$ . By considering again the EKV model, the initial conditions can be determined by solving the following algebraic equation:

$$\frac{x}{L} \left\{ r_s(L,0) + \left( \theta - \frac{1}{K_2(0)} \right) \frac{r_s^2(L,0)}{2} - \frac{\theta r_s^3(L,0)}{3K_2(0)} \right\} + \left( 1 - \frac{x}{L} \right) \left\{ r_s(0,0) + \left( \theta - \frac{1}{K_2(0)} \right) \frac{r_s^2(0,0)}{2} - \frac{\theta r_s^3(0,0)}{3K_2(0)} \right\} = r_s(x,0) + \left( \theta - \frac{1}{K_2(0)} \right) \frac{r_s^2(x,0)}{2} - \frac{\theta r_s^3(x,0)}{3K_2(0)} \quad (9)$$

The channel terminal currents can be established through the integration of Eq.(1). These currents take the forms:

$$I_S(t) = I_{avr}(t) + \theta N_\rho C_{ox} V_T wL \frac{d}{dt} \int_0^1 (1-\xi) r_s(\xi,t) d\xi \quad \xi \triangleq \frac{x}{L} \quad (10)$$

$$I_D(t) = I_{avr}(t) - \theta N_\rho C_{ox} V_T wL \frac{d}{dt} \int_0^1 \xi r_s(\xi,t) d\xi \quad (11)$$

In these expressions,  $I_S(t)$  is the dynamic source current,  $I_D(t)$  is the dynamic drain current, whilst  $I_{avr}(t)$  denotes the average channel current. In terms of EKV model,  $I_{avr}(t)$  can be calculated as:

$$I_{avr}(t) = -\theta \mu_0 \frac{K_1 V_T^2 N_\rho C_{ox} w}{K_2} \left\{ r_s(L,t) - r_s(0,t) + \left( \theta - \frac{1}{K_2} \right) \left( \frac{r_s^2(L,t) - r_s^2(0,t)}{2} \right) - \frac{\theta}{K_2} \left( \frac{r_s^3(L,t) - r_s^3(0,t)}{3} \right) \right\} \quad (12)$$

Additionally, the gate current  $I_G(t)$  is the oxide capacitance current and has a formula given by:

$$I_G(t) = I_{offG}(t) - wLC_{ox} \frac{d}{dt} \left( \theta V_T \int_0^1 r_s(\xi,t) d\xi + V_G(t) - V_B(t) - \psi_p \right) \quad (13)$$

In the preceding relation,  $I_{offG}(t)$  denotes the offset gate current resulting from the probability of gate tunneling. According to EKV model, this current can be evaluated with the aid of:

$$I_{offG}(t) = - \frac{K_G \theta N_\rho V_T^2 wL}{t_{ox}^2} \int_0^1 r_s(\xi,t) v_{ox} P_{tun}(v_{ox}) d\xi \quad (14)$$

where

$$v_{ox} \triangleq 2N_\rho (r_s(\xi,t) + r_{fc}) + \gamma_b \sqrt{\frac{\psi_p}{V_T} - \theta r_s(\xi,t)} \quad (15)$$

and

$$P_{tun}(v_{ox}) \triangleq \begin{cases} \exp \left\{ -\frac{E_B t_{ox}}{v_{ox} V_T} \left[ 1 - \left( 1 - \frac{v_{ox} V_T}{X_B} \right)^{3/2} \right] \right\} & \text{for } v_{ox} \leq \frac{X_B}{V_T} \\ \exp \left( -\frac{E_B t_{ox}}{v_{ox} V_T} \right) & \text{otherwise} \end{cases} \quad (16)$$

In this set of formulas,  $P_{tun}$  stands for the tunneling probability,  $X_B$  is the oxide-channel voltage barrier,  $E_B$  denotes the characteristic electric field,  $t_{ox}$  is the oxide thickness,  $\psi_p$  is the pinch-off surface potential,  $r_{fc}$  symbolizes

the fixed normalized charge density,  $\gamma b$  is the normalized body effect coefficient,  $KG$  is the gate tunneling current mobility multiplied by  $Cox$ , and  $v_{ox}$  is the normalized oxide voltage. Finally, the bulk current  $I_B(t)$  can be obtained through the application of the charge conservation principle. The result of this application yields:

$$I_B(t) = - [I_S(t) + I_D(t) + I_G(t)] \quad (17)$$

### III. OVERVIEW ON THE CUBIC SP-LINE COLLOCATION METHOD

The sp-line collocation method is a piecewise approach to solve the continuity equation which is a function of the normalized channel charge density. It is one dimensional second order spatially and first order temporally partial differential equation that describes the transient state of the MOS transistor. The strategy of this technique is to divide the channel length into equal limited number of segments such that the continuity equation solution for each segment can be represented as a sum of products of distinct functions of time and position. These model parameters depend on the normalized channel charge density at the collocation points and channel bounds. This dependence, of model parameters, limits the required number of segments because shortening the segments makes the segment modelling more dependent on the normalized density at channel bounds as the segmentation method [13]. The modelled solution coincides with the real solution at the collocation points necessitating mathematical interpolation between these points to be achieved. This obligates the piecewise models to keep spatial continuity up to the second derivative and to take into account the physical conditions that nullify the spatial second derivative at the channel bounds in accordance with the continuity equation. As a result, the model parameters need a set of algebraic equations, the size of which is four times the number of segments, to be determined in terms of normalized densities at the collocation points and channel bounds. After that, a system of ordinary differential equations, of size equal to the number of collocation points, is required to be solved in order to determine the normalized charge densities at these points. To sense the transient event, the segment length is defined as the distance travelled by an electron, with a velocity resulted from the literal electric field caused by the drain-source voltage, in a time interval of duration of tenth [10] of that of the transient action. Because of the normalized channel charge density is graduated and of bounded values, it can be spatially modelled as a cubic polynomial to match the number of algebraic equations. The solution of the resulting equations determines the model parameters. This interpolation is called cubic sp-line collocation method. Due to the importance of this procedure, we are going to outline its basic background. The starting formula is associated with the number of segments  $N$  which is given by:

$$N = \sqrt{\frac{10L^2S}{\mu_0 V_{DS}}} \quad (18)$$

$S$ , in the above formula, denotes the slope of the transient action,  $\mu_0$  is the low field mobility,  $L$  is the channel length, and  $V_{DS}$  is the drain-source voltage. The segment length must not be less than the depletion width  $x_d$  that is defined as:

$$x_d \triangleq \sqrt{\frac{4\phi_F \varepsilon_{si}}{q N_b}} \quad (19)$$

In this mathematical expression,  $\phi_F$  denotes the Fermi potential,  $q$  is the electron charge,  $\varepsilon_{si}$  represents the silicon permittivity, and  $N_b$  stands for the substrate doping. For  $N$  segments, the cubic model for the  $n^{th}$  segment is determined by:

$$\begin{aligned} r_s(\xi, t) = & n r_s\left(\frac{n-1}{N}, t\right) - (n-1) r_s\left(\frac{n}{N}, t\right) - n(n-1) a_{2(n-1)} + \\ & \xi \left( N r_s\left(\frac{n}{N}, t\right) - N r_s\left(\frac{n-1}{N}, t\right) + (2n-1) N a_{2(n-1)} - n(n-1) a_{2n-1} \right) \\ & + \left( N(2n-1) a_{2n-1} - N^2 a_{2(n-1)} \right) \xi^2 - N^3 a_{2n-1} \xi^3 \quad \& \quad \frac{n-1}{N} \leq \xi \leq \frac{n}{N} \end{aligned} \quad (20)$$

Note that,  $r_s(\xi, t)$  is the normalized inversion charge density as a function of normalized channel position,  $\xi$ , and time,  $t$ . Additionally, the continuity conditions for  $m^{th}$  collocation point is calculated as:

$$a_{2m} = -(m-1)(2r_m - r_{m-1} - r_{m+1}) + (2m-1)a_{2(m-1)} + \left(\frac{2m^2}{N}\right)a_{2m-1} \& r_m \triangleq r_s\left(\frac{m}{N}, t\right) \quad (23)$$

$$a_{2m+1} = N(2r_m - r_{m-1} - r_{m+1}) - 2N a_{2(m-1)} - (2m+1) a_{2m-1} \quad (22)$$

Moreover, the natural conditions at the channel bounds are determined with the aid of:

$$a_1 = N a_0 \quad \& \quad -(N+1) a_{2N-1} = N a_{2(N-1)} \quad (23)$$

By solving the set of algebraic equations, Eqs.(21-23), the model parameters  $a_0$  to  $a_{2N-1}$  can be computed. The performance of this method is poor, as it is applied to a physical based MOS model such as EKV, since it ignores the realization of natural conditions for any of its sides across the channel length. This ignorance means that the spatial first partial derivative of the normalized channel charge density is graded along the channel. This reality alters the accuracy of the model much more than enlarging the degree of continuity of the segments models when dealing with a charge based compact model like EKV model. So, some supplementary improvements are still required in order to solve the previously illustrated problems which are associated with the cubic sp-line collocation method.

### IV. SYMMETRICAL TELESCOPIC MODIFICATION ON THE CUBIC SP-LINE COLLOCATION METHOD

To solve the problem of natural condition realization, it is easy to create a telescopic cubic sp-line collocation algorithm. Initially, this procedure estimates the number of segments using usual sp-line collocation algorithm and then applying cubic sp-line collocation on a sub-channel with a length starting from one of the segment and ends at one of the channel bounds. Of course, the collocation points nearer to the source will have sp-line collocation with respect to drain and vice versa. This will be taken into account in order to include more collocation points. So, half of the collocation points will be referred to the source and the other will be referred to the

drain and hence the telescopic modelling will be symmetrical. For an odd segmented channel, the segment includes the half point of the channel length will be split into two halves; each half will be modelled referring to the more far end. Our proposed modification to the cubic sp-line collocation method magnifies its sensitivity to the normalized position,  $\xi$ , which is very high for small channel lengths. In addition, the decreasing of the drain-source voltage will enlarge the effect of the boundary channel normalized charge density on the interpolation processes. The LDR power transistor is characterized by small channel length and low drain-source voltage. As a consequence, it is suggested that partitioning the LDR output transistor into just one segment will be sufficient enough to model its transient mode using our modified collocation method. Our novel algorithm of the usual collocation method is validated on an NMOS power transistor that is characterized by the data given in Table I.

TABLE I  
CHARACTERISTICS OF THE EXAMINED NMOS POWER TRANSISTOR

Simulation Settings		Value
CMOS technology		standard 0.18 $\mu\text{m}$ [14-15]
Simulator		MATLAB R2014a
Solver		pdepe
Channel length		0.46 $\mu\text{m}$
Time duration of simulation $t$		5nsec
drain voltage, $V_D$		0.1V
Number of spatial axis exact solution points		Equally spaced 61 points from source to drain
Number of temporal axis exact solution points		Equally spaced 1001 points from start to the end of the simulation time
Number of collocation points		0
Source voltage, $V_S$		0V
Bulk voltage, $V_B$		0V
Gate voltage, $V_G$	Overshot case	$10^{10}tV$ for $t \leq 0.1\text{nsec}$ $0V$ Otherwise
	Undershot case	$1-10^{10}tV$ for $t \leq 0.1\text{nsec}$ $1V$ Otherwise

The power transistor channel length is nearly ten times the depletion width in order to ensure appropriate shortening that length to realize small area transistor without suffering from the short channel effects. Fig.(1) illustrates the exact and the modelled solution in the form of time sweep at values of  $\xi = \{55/60, 56/60, 58/60, 59/60\}$ . These values of  $\xi$  are chosen to be very near to the drain to demonstrate the validity of our motivated model for the worst case. The normalized charge density close to the drain deteriorates so fast that most of the interpolative models can't track the exact solution. The original normalized charge density obtained from the actual solution of the continuity equation is denoted by  $r_s$  while the modelled one is symbolized by  $r_{sc}$ . Fig.(2) illustrates the same thing as Fig.(1) but for the situation of downward ramping. Both of these figures demonstrate the evidence of coincidence between the identified solution and the true one.

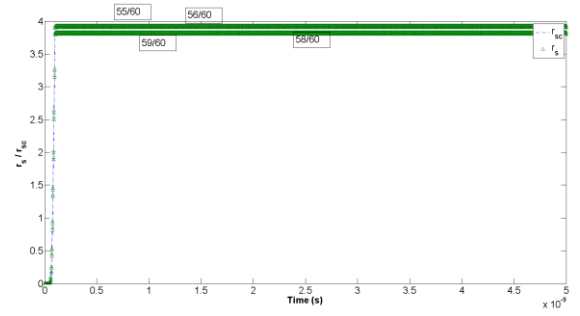


Fig. 1.  $r_s(t)$  and  $r_{sc}(t)$  at  $\xi = \{55/60, 56/60, 58/60, 59/60\}$  for NMOS,  $L = 0.46\mu\text{m}$ ,  $N = 1$ ,  $V_{SD} = 0.1\text{ volt}$ , the input is upward ramp with  $S = 10\text{Gvolt/sec}$  and  $V_{PP} = 1\text{ volt}$ .

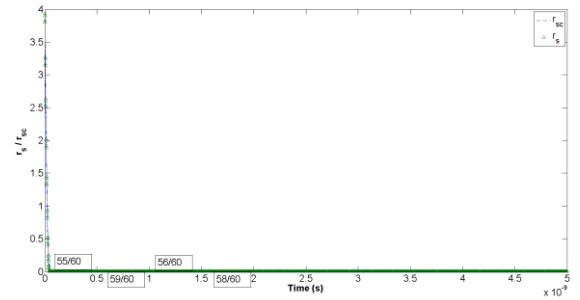


Fig. 2.  $r_s(t)$  and  $r_{sc}(t)$  at  $\xi = \{55..59/60\}$  for NMOS,  $L = 0.46\mu\text{m}$ ,  $N = 1$ ,  $V_{SD} = 0.1\text{ volt}$ , the input is downward ramp with  $S = -10\text{Gvolt/sec}$  and  $V_{PP} = 1\text{ volt}$ .

## V. THE PROPOSED METHODOLOGY

Our methodology concentrates basically on dealing with the idea of designing the LDRs under impact of transient loading from the power transistor point of view. The power transistor is supposed to be free of body effect. This is done by connecting the transistor source to its body in order to avoid the complication of the transient currents computations. Our procedure considers only the load transient regulation of the NMOS power transistor of negative LDR. As a result, the only controlling parameters of the power transistor in the transient mode are the gate and drain voltages as well as current. The transient currents are functions of transient terminal voltages as depicted from our proposed transient model mentioned later. This transient procedure is used with the coincidence of EKV model and applied to the LDR power transistor through the following set of equations given that the source voltage is unchanged.

$$I_D(t) = I_{avr}(t) - \theta C_{ox} N_p V_T w L \frac{d}{dt} \left( \frac{r_s(0,t)}{6} + \frac{r_s(L,t)}{3} \right) \quad (24)$$

$$I_G(t) = -wLC_{ox} \frac{d}{dt} (0.5\theta V_T (r_s(0,t) + r_s(L,t)) - V_G - \psi_p) \quad (25)$$

$$V_{th} = V_{fb} + 2\phi_F + V_{sh} + \frac{\Gamma^2}{2} \left( \xi_c \left( 1 - \frac{N_b}{N_{bch}} \right) + \sqrt{\left( \xi_c \frac{N_b}{N_{bch}} \right)^2 - \frac{N_b}{N_{bch}} \left( \xi_c^2 - \frac{8\phi_F + 4V_{sh}}{\Gamma^2} \right)} \right) + \frac{\Gamma^2}{\Gamma_g^2} (2\phi_F + V_{sh}) - \frac{\Gamma \rho_{fc}}{\Gamma_g^2 C_{ox}} \sqrt{2\phi_F + V_{sh}} \quad (26)$$

$$\sqrt{\psi_p} = \frac{\Gamma_g}{2(\Gamma^2 + \Gamma_g^2)} \left( \sqrt{4(\Gamma^2 + \Gamma_g^2)(V_G - V_B - V_{fb}) + (\Gamma_g)^2} - \Gamma_g \right) \quad (27)$$

$$K_1 = 0.0215625 \theta C_{ox} N_p T \left\{ 0.5 - (1 + 2\Gamma^{-1} \sqrt{\psi_p})^{-1} \right\}^{-1} \quad (28)$$

$$K_2 = K_1 + 23188.4058 T^{-1} \psi_p (1 + 2\Gamma^{-1} \sqrt{\psi_p})^{-1} \quad (30)$$

$$V_{sh} = 8.625 \times 10^{-5} T \ln(4 N_p \Gamma^{-1} \sqrt{\psi_p}) + 1.120705143 \times 10^{-7} \sqrt[3]{N_{bch} \psi_p} \quad (31)$$

$$\frac{dr_s(0/L,t)}{dt} = \frac{dr_s(0/L,t)}{dv(0/L,t)} \times \frac{dv(0/L,t)}{dt} \Delta h(r_s(0/L,t)) \frac{dv(0/L,t)}{dt} = \left\{ r_s(0/L,t)^{-1} + 2 \right\}^{-1} \frac{dv(0/L,t)}{dt} \quad (32)$$

$$\frac{dv(0,t)}{dt} = \frac{1}{N_v V_T} \left( \frac{dV_G}{dt} - \frac{dV_{th}}{dt} \right) \quad (33)$$

$$\frac{dv(L,t)}{dt} = \frac{1}{N_v V_T} \left( \frac{dV_G}{dt} - \frac{dV_{th}}{dt} \right) - \frac{dV_D}{dt} \quad (34)$$

$$\frac{dV_{th}}{dt} = \left( \frac{dV_{th}}{dV_{sh}} \right) \left( \frac{dV_{sh}}{d\psi_p} \right) \left( \frac{d\psi_p}{dt} \right) \quad (35)$$

$$\frac{dV_{th}}{dV_{sh}} = 1 + \frac{N_b}{N_{bch}} \left\{ \left( \xi_c \frac{N_b}{N_{bch}} \right)^2 - \left( \frac{N_b}{N_{bch}} \right) \left( \xi_c^2 - \frac{8\phi_F + 4V_{sh}}{\Gamma^2} \right) \right\}^{-0.5} + \left( \frac{\Gamma}{\Gamma_g} \right)^2 - \frac{\Gamma \rho_{fc}}{\Gamma_g^2 C_{ox}} \{ 2\phi_F + V_{sh} \}^{-0.5} \quad (36)$$

$$\frac{dV_{sh}}{d\psi_p} = 4.3125 \times 10^{-5} \psi_p^{-1} T + 3.7356838 \times 10^{-8} \left\{ \frac{\psi_p^2}{N_{bch}} \right\}^{\frac{1}{3}} \quad (37)$$

$$\frac{d\psi_p}{dt} = g(\psi_p) \frac{dV_G}{dt} = \left\{ 1 + \left( \frac{\Gamma}{\Gamma_g} \right)^2 + \frac{\Gamma}{2\sqrt{\psi_p}} \right\}^{-1} \frac{dV_G}{dt} \quad (38)$$

In the above mathematical formulas, the different parameters are defined as:

$\Gamma_g$  is the depletion factor in the poly-silicon gate.

$N_b$  is the doping concentration of the substrate.

$\rho_{fc}$  is the Fixed charge density.

$N_{bch}$  is the channel doping concentration of the substrate.

$V_{fb}$  is the flat-band voltage.

$\xi_c$  is the normalized characteristic depth.

The controlling parameters of the studied power transistor and/or their temporal derivatives can form a system of two differential equations. The resulting equations can be complicated as we desire, on the cost of hardness of hardware realization. In addition, the parameters included in the equations are so hard to be optimized. Generally, the goal of the system of equations is the stabilization of the LDR output which is the drain voltage of the power transistor. Under the impact of loading, the nominal output value must be rapidly restored keeping low power consumption and allowable voltage ranges. There are some notes that can facilitate the evaluation of the higher degrees of the temporal derivatives of terminal currents. The first one of them is that the temporal derivative of the normalized inversion charge density can be formed in terms of charge density and terminal voltages as Eq.(31) demonstrates. This will allow us to use the built in inverse of Eq.(7 or 8) in the simulator or any proposed inverse function directly. The second notation is that the threshold voltage is a nested function of the EKV model parameters. Because of this, the determination of the temporal derivative can be easily achieved through the use of chain rule. The details of this problem is outlined in our APPENDIX. For the sake of simplicity, we will suppose a simple second order system depending on cross-coupling control between the gate and drain voltages as well as currents and the input of which is the load current. This system is described by the following set of equations:

$$I_R = I_D - I_L \quad (39)$$

$$\frac{d^2 V_G}{dt^2} = a_1 I_R \quad (40)$$

$$\frac{d^2 V_D}{dt^2} = a_2 I_G \quad (41)$$

Where  $I_L$  denotes the load current,  $a_1$  &  $a_2$  are the parameters of the proposed system of equations.

The parameters of these mathematical formulas are optimized to attain the aimed goals of our methodology. This cross coupled system is the simplest that can be proposed as the terminal voltage can't be controlled by its own current in the transient mode. We have chosen a second order system, as the least order, to include the probability of oscillation for some parameters and to realize bounding of some parameters in the allowed limits.

## VI. MODEL ASSESSMENT SIMULATION RESULTS

In this section, we are going to simulate our proposed model to see its validity for practical applications. Our simulation results are given for the system parameter values that are indicated in Table II. It is of importance to notice that the switched parameters  $a_1$  and  $V_G(0)$  change their state according to the load current transition case. This switching action matches with the load current transition mechanism which is actually based on the switching of the loads. These loads represent the power managed circuits of the LDR. Taking into account this action, an abruptly changing of the

load current signifies switching events. As a consequence of this, it is logical to assume switching mechanisms for some parameters or initial conditions. In this regard, the load current transition can be determined as:

TABLE II  
SYSTEM PARAMETER VALUES

Simulation Settings		Value
Power transistor		NMOS
CMOS technology		0.18 $\mu\text{m}$ [14-15].
$V_B$		-1V
$V_S$		-1V
$T$		300K
$w$		9000 $\mu\text{m}$ .
$L$		0.46 $\mu\text{m}$
$I_L$		[0,0.1]A
$S$		$2 \times 10^{11}$ A/sec
Time duration of all simulations $t$		$10^4$ sec
$r_s(0/L,t)$ calculation in terms of terminal voltages		using MATLAB 2014a defined inverse function "lambertw".
Solver		ode23tb
In case of overshoot.	$a_1$	-0.01
	$a_2$	1
	$V_G(0)$	0
	$V_D(0)$	-0.9
	The remaining initial conditions	0
In case of undershoot.	$a_1$	0.01
	$a_2$	1
	$V_G(0)$	-0.9
	$V_D(0)$	-0.9
	The remaining initial conditions	0

$$I_L = I_{L_f} - (I_{L_f} - I_{L_i})e^{-St} \quad (42)$$

In the preceding formula,  $I_{L_f}$  denotes the final value of the load current transition,  $I_{L_i}$  represents the initial value of the load current transition, and  $S$  is the transition scaling factor.

The behaviour of the load transition is supposed to be represented as an exponential sweep starting from its initial value till its final value with sweeping width equal to the range of the load current. This exponential representation of the load transient is chosen to facilitate the differentiation of the load currents without trapping into temporal jumps of derivatives. The channel length of the LDR power transistor is selected in order of ten times the depletion width to be able to derive large amount of load currents keeping avoidance of the short channel effects [12]. Fig.(3) depicts the dynamic gate voltage in the case of load current overshoot. The displayed results of this plot shows its oscillation within a small range of mV. The deviation of the output voltage from the initial value in this transition situation is illustrated in Fig.(4). Regarding to this

graph, it is noted that there is an instability increasing case. However, having a look on the amount of temporal deviation, it is found that its value is in order of  $\mu\text{V}$  during a time of about 104 sec. This allows the small signal noise suppression techniques to easily restore the nominal value of the output voltage. Fig.(5) displays the gate current for overshoot state of the load current transition. The gate current oscillatory varies in very low range in order of parts of nA. The difference between the drain and load currents in case of upward jump is traced in Fig.(6). It is turned out to note that there is a quasi impulse at the initial time point and then instantaneously starting to oscillate in the ranges of hundreds of  $\mu\text{A}$ . Fig.(7) demonstrates the difference between these two currents excluding the initial impulse during that load jumping. This plot represents a zooming of Fig(6) by excluding its jump event to allow the observation of the way in which the current varies. On the other hand, the deviation of the output voltage from initial value in the case of undershoot is displayed in Fig.(8). This scene shows the same results that are plotted in Fig(4) with the exception that the output voltage is decreasingly varying. Fig.(9) exhibits the dynamic gate voltage in downward transition of the load current. A big insight into the behaviour of this plot, it is noted that the gate voltage degenerates by a range of about -0.2 volts during the specified simulation time. The very slow variation rate illustrated by this graph allows the small signal stabilization procedure to adjust the gate voltage. The gate current in the state of down jumping is demonstrated in Fig.(10). This current has initial jumps and then it stabilizes, in quasi no time, at a value characterized by very small ranges of tenths of nA. This will allow the gate current to restore its nominal zero average value. Fig.(11) manifests the difference between the drain and load currents in the state of downward transition. It is evident that there is a jump at the initial time point and then an instantaneous decaying to the values in the order of nA. The demonstration that is expressed in Fig.(7) for the upward transition is introduced for the opposite situation in Fig.(12). This figure allows the notation of the temporal variation of the current that is demonstrated in Fig(11). That current is very important as it will feed the regulator circuit and it can be taken as a very basic indicator for the regulator power consumption. In spite of rather high difference between the load and drain currents in the case of overshoot, it is still less than 0.1% of the load current and this is an allowable range for restoring LDR steady state conditions. All of the introduced results illustrate that our proposed methodology introduces an LDR of a quasi insensitive response to load current transitions along with keeping low power consumption. This is achieved using a systematic transient approach with the ability of model parameters tolerating.

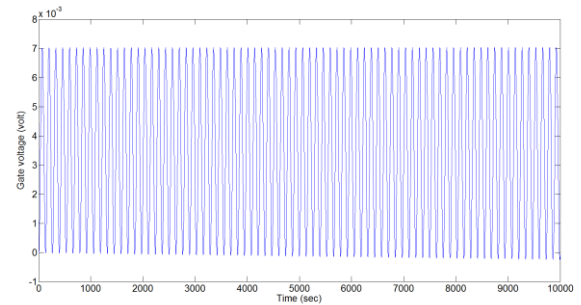


Fig. 3. Dynamic gate voltage in case of overshoot

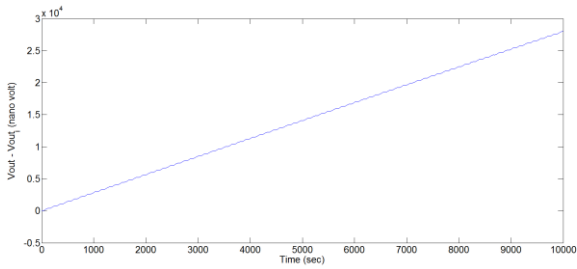


Fig. 4. Deviation of the output voltage from initial value in case of overshoot

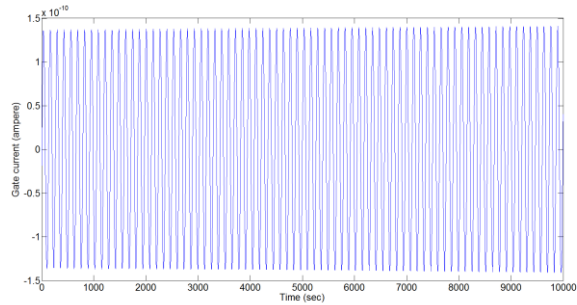


Fig. 5. Gate current in case of overshoot

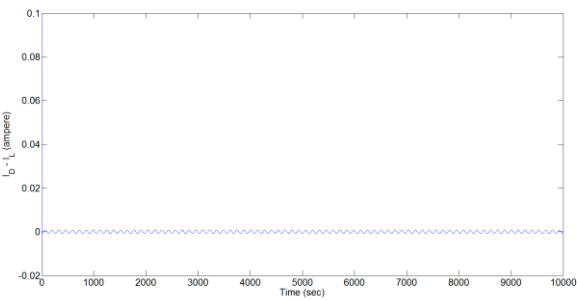


Fig. 6. Deviation of the drain current and load current in case of overshoot

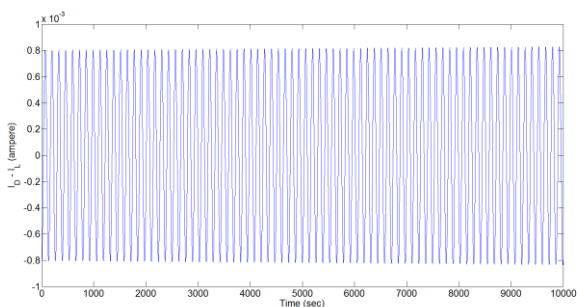


Fig. 7. Difference of the drain current and load current excluding the initial jump in the case of overshoot

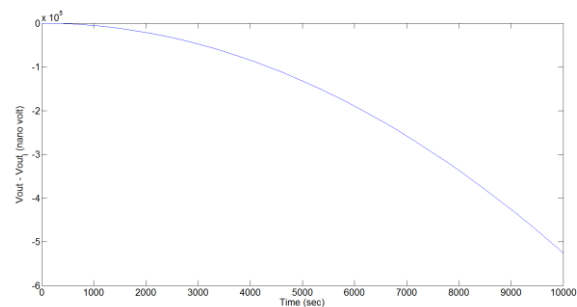


Fig. 8. Deviation of the output voltage from initial value in the case of undershoot

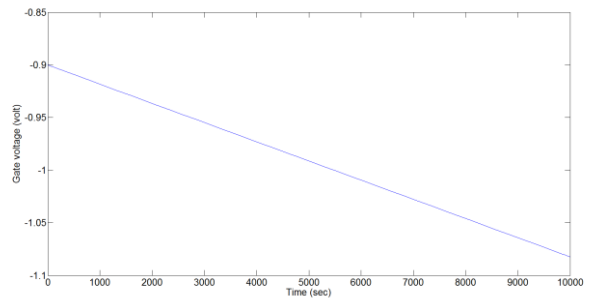


Fig. 9. Dynamic gate voltage in undershoot case

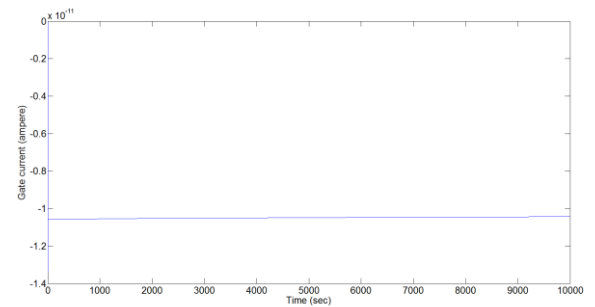


Fig. 10. Gate current in undershoot situation

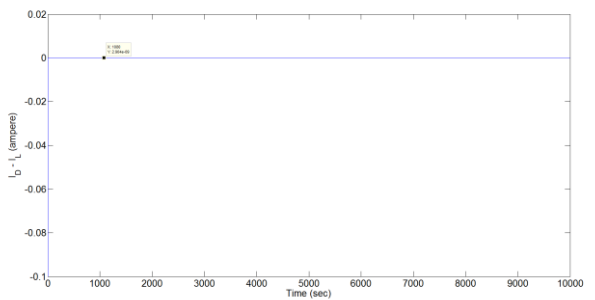


Fig. 11. Difference between the drain and load currents in case of undershoot

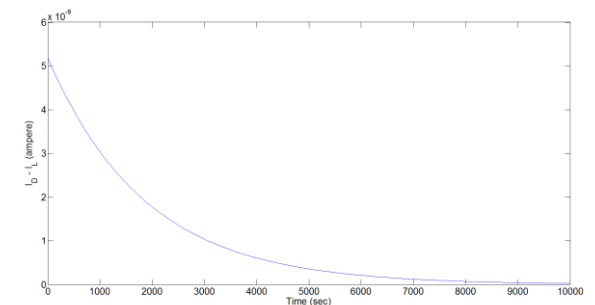


Fig. 12. Difference between the drain and load currents excluding the initial jump in undrshot case

VII. CONCLUSIONS

In this paper, we proposed a new methodology that motivates the transient regulation of LDR's depending on the real transient model of MOS device. To our knowledge, this is the first time that the problem of the load transient impacts is treated independently upon the other stability settings for the LDR. In contrast of the situation of the previously published

works [1-9], the impact loading is no more considered as a supplementary item in the design flow of the LDRs. Proving this methodology creates a frame of realizing circuits to treat this problem taking into account that the complete actual model of the MOS transient terminal currents are represented by the continuity equation. The cross-coupling control between gate and drain voltages as well as currents achieves the regulation function with low power consumption. This is accomplished under constrain of switched biasing that is controlled by switching loads to provide the convenient initial conditions. Our results demonstrates that the symmetrical telescopic modification of the cubic sp-line collocation procedure is much more efficient and simple model than the previously introduced procedures for the transient response of the LDR power transistor. Additionally, charge based model, such as EKV model, gives the ability of nested functions for the parameters of the model equations which gives us the ability of developing the methodology. Moreover, under the existence of the small signal noise suppression techniques, the instability of the output voltage, with very slow variation, can be remedied by these techniques. As a final conclusion, it is evident that realizing extremely slow instability is sufficient for the LDR process to be stabilized using the preceding mentioned techniques.

#### APPENDIX A

##### Some Useful Formulas For The Developing Of The Proposed Methodology

$$\frac{d^n h(r_s(0/L, t))}{dr_s(0/L, t)^n} = 2^{n-2}(n-1)! \{-1 + r_s(0/L, t)\}^{-n} \quad \text{for } n > 1 \quad (\text{A1})$$

$$\frac{d^n V_{sh}}{dV_{sh}^n} = \left\{ \frac{N_b}{N_{bch}} \left\{ \left( \xi_c \frac{N_b}{N_{bch}} \right)^2 - \left( \frac{N_b}{N_{bch}} \right) \left( \xi_c^2 - \frac{8\phi_F + 4V_{sh}}{\Gamma^2} \right) \right\}^{0.5-n} \right\} - \left\{ \prod_{k=2}^n 1.5-k \text{ for } n > 1 \right. \\ \left. \frac{\Gamma \rho_{fc}}{\Gamma_g^2 C_{ox}} \{2\phi_F + V_{sh}\}^{0.5-n} \right\} \quad (\text{A2})$$

$$\frac{d^n V_{sh}}{d\psi_p^n} = \psi_p^{-n} \left( 4.3125 \times 10^{-5} T(-1)^{n-1} (n-1)! + 3.7356838 \times 10^{-8} \sqrt{N_{bch} \psi_p} \prod_{k=2}^n \frac{4}{3} - k \right) \quad \text{for } n > 1 \quad (\text{A3})$$

$$\frac{d^n g(\psi_p)}{d\psi_p^n} = \sum_{m=1}^n P_m g^m(\psi_p) \psi_p^{-\frac{2n+m-3}{2}} \left\{ \frac{\Gamma}{2} \right\}^{m-1} \quad (\text{A4})$$

$$\frac{d^n K_1}{d\psi_p^n} = -\frac{185.5072463}{\theta C_{ox} N_p T} \sum_{m=1}^{n+1} P_m g_2^m(\psi_p) \psi_p^{-\frac{2n+m-1}{2}} \left\{ \frac{\Gamma}{2} \right\}^{m-1} \quad (\text{A5})$$

$$\frac{d^n K_2}{d\psi_p^n} = \frac{d^n K_1}{d\psi_p^n} - \frac{23188.4058}{T} \left\{ P_m g_2^m(\psi_p) \psi_p^{-\frac{2n+m-1}{2}} \left\{ \frac{\Gamma}{2} \right\}^n + \left( n + \psi_p^2 \right) \sum_{m=1}^n P_m g_2^m(\psi_p) \psi_p^{-\frac{2n+m-3}{2}} \left\{ \frac{\Gamma}{2} \right\}^{m-1} \right\} \quad (\text{A6})$$

$$g_1(\psi_p) = \left\{ 1 + \frac{\Gamma}{2\sqrt{\psi_p}} \right\}^{-1} \quad (\text{A7})$$

$$g_2(\psi_p) = \left\{ -1 + \frac{\Gamma}{2\sqrt{\psi_p}} \right\}^{-1} \quad (\text{A8})$$

$$F = [f_{ij}] \quad \begin{cases} f_{i-1j} - f_{i-1j-1} & \text{for } 3 \leq i \leq n \ \& \ 2 \leq j \leq i \\ 1 & \text{for } i = 2 \ \& \ j = 2 \\ 0 & \text{otherwise} \end{cases}$$

$$F_d = [f_{dij}] \quad \begin{cases} \max(f_{i-1j}, f_{i-1j-1}) & \text{for } j > \frac{i+2}{2} \\ f_{ij} - \max(f_{i-1j}, f_{i-1j-1}) & \text{otherwise} \end{cases}$$

$$F_e = [f_{ej}] \quad \begin{cases} f_{ij} - \max(f_{i-1j}, f_{i-1j-1}) & \text{for } j > \frac{i+2}{2} \\ \max(f_{i-1j}, f_{i-1j-1}) & \text{otherwise} \end{cases}$$

$$G_d = [g_{dij}] \quad \begin{cases} \frac{(-1)^i}{2} (j-1) f_{dij} \\ G_e = [g_{ej}] \\ g_{ej} = \frac{(-1)^{i-1}}{2} \left( \frac{2(i-1) + j - 1}{2} \right) f_{ej} \end{cases}$$

$$Q = [q_{ij}]$$

$$q_{ij} = \begin{cases} g_{ej} q_{i-1j} + g_{dij} q_{i-1j-1} & \text{for } 4 \leq i \leq n \ \& \ 2 \leq j \leq i \\ 1 & \text{for } i = 1 \ \& \ j = 1 \\ 0.5 & \text{for } i = 2 \ \& \ j = 2 \\ g_{e32} + g_{d32} & \text{for } i = 3 \ \& \ j = 2 \\ g_{e33} + g_{d33} & \text{for } i = 3 \ \& \ j = 3 \\ 0 & \text{otherwise} \end{cases}$$

$$P = [p_j] \quad p_j = q_{nj} \quad (\text{A9})$$



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