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Switching-mode audio amplifier based on a ΔΣ A/D converter

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***Abstract*—The article describes the design and implementation of a modular hardware platform intended for testing and measuring various configurations of switching-mode audio amplifiers based on sigma-delta modulation. Two single-channel power amplifier modules were designed and manufactured, along with a stereophonic module serving as the basic source of modulated signals. Additionally, measurements were conducted on the fundamental parameters of the completed amplifier, such as harmonic distortion level, dynamic range, and output power. The developed platform serves as a foundation for modifications and further advancement in the technology of building switching-mode audio amplifiers.**

***Keywords*—Acoustic amplifier; Switching-mode amplifier; Digital amplifier; ΔΣ modulation; Class D**

I. Introduction

SWITCHING - mode acoustic amplifiers, also known as digital or class D amplifiers, can be found in many of the devices we use every day. Starting from portable music players that were popular not so long ago, through mobile phones, audio-visual systems, and ending with stage equipment. They are used wherever low power consumption, low power lost in the form of heat or, in the case of devices with high output power, keeping their dimensions and weight as small as possible are critical.

The origins of this technology date back to the 1950s, but the lack of transistors with appropriate parameters prevented its practical use for the next 30 years. Modern switching-mode amplifiers achieve such good parameters that they are increasingly often implemented in Hi-Fi devices.

The motivation for the project described in this work is an attempt to further develop the technology of switching-mode acoustic amplifiers by diverting from the commonly used pulse width modulation (PWM) in favour of ΔΣ modulation.

The aim of the described project is to design and implement a modular hardware platform supporting measurements of various configurations of impulse audio amplifiers. The amplifiers will be implemented using ΔΣ modulation. The hardware platform will also enable listening tests of designed amplifier configurations.

II. ΔΣ Modulation

In the simplest form, a ΔΣ modulator consists of an integrator, comparator, and a negative feedback loop. The signal supplied to the input is delayed by the integrator and coarsely quantized by the comparator [1]. The introduced error is then subtracted from the input signal by the feedback loop in attempt to correct it in the next cycle. Figure 1 shows simplified structure of an analogue 1-bit ΔΣ modulator.

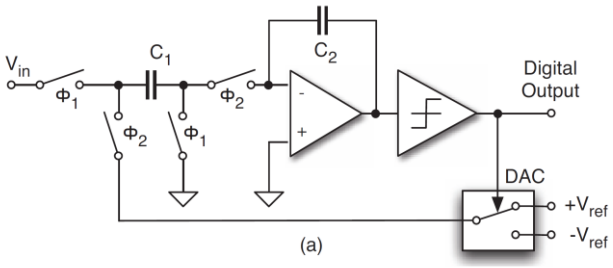

Fig. 1. Simplified structure of an analogue 1-bit ΔΣ modulator

The 1-bit ΔΣ modulator produces on its output a stream of pulses with average density proportional to the level of the supplied signal, as shown in Fig. 2.

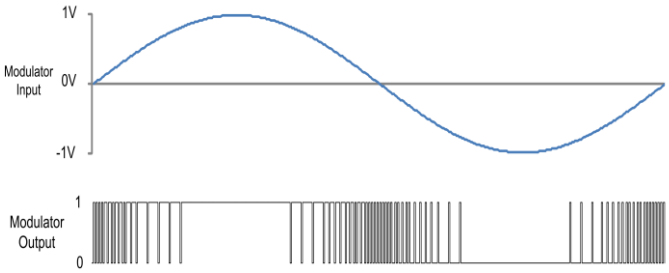

Fig. 2. Sine wave input (top) and modulated output bit stream (bottom)

The closer input signal is to the maximal value, the more '1' bits are on the output of the modulator. On the other hand, when the input signal approaches the minimal value, '0' bits become more frequent.

Significant advantage of ΔΣ modulation over the PWM is spectral shaping of the quantisation noise in such a way that most of its energy is shifted above the acoustic frequency range. The steepness of the noise shaping curve depends on the modulator's order, i.e. number of integrators in the structure. Figure 3 shows the noise spectral density for modulators of different orders.

The reason of this phenomenon is that the quantisation noise is fed back to the modulator's input. The limited passband of the integrator prevents the noise suppression in high-frequency range [1].

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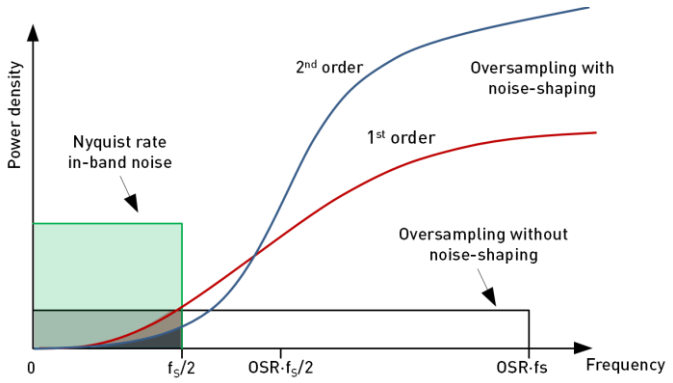

Fig. 3. Noise shaping in ΔΣ modulators

The principle of operation of typical PWM modulators is feeding the analogue signal and a generated internally triangle wave into the analogue comparator. Figure 4 shows simplified structure of such modulator.

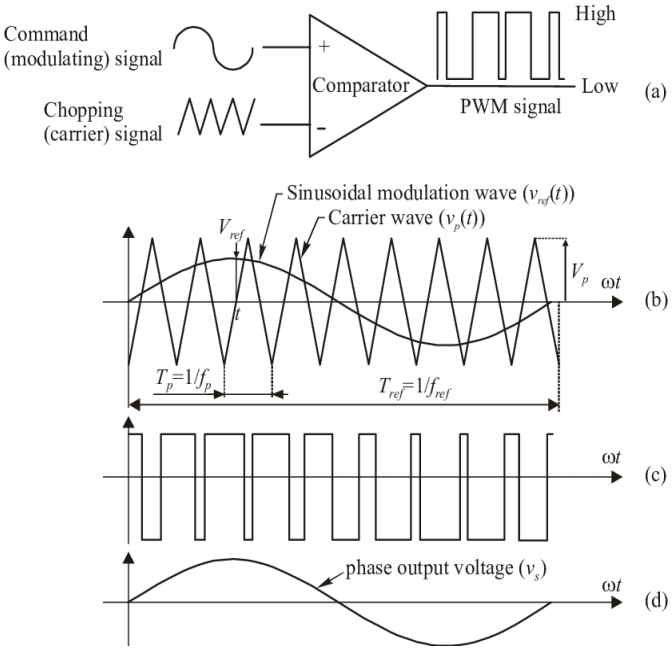

Fig. 4. Simplified structure of a PWM modulator (a), sinusoidal and carrier wave (b), PWM output signal (c) and extracted low-frequency component (d)

As shown above (Fig. 4.), PWM modulators do not utilize the negative feedback loop, which means that achieving satisfactory accuracy is often challenging.

III. Proposed Class-D Amplifier

The main engineering problem that this work focuses on is the design and implementation of a high-frequency output stage of a switching power amplifier. To effectively drive the loudspeakers, this system must be characterized by high operating speed, low switching losses and appropriate current capacity.

A secondary role is played by supporting systems, the presence of which is necessary for the proper operation of the entire device or the safety of its use. These systems have been designed in such a way that they fulfill their role with the least possible complexity.

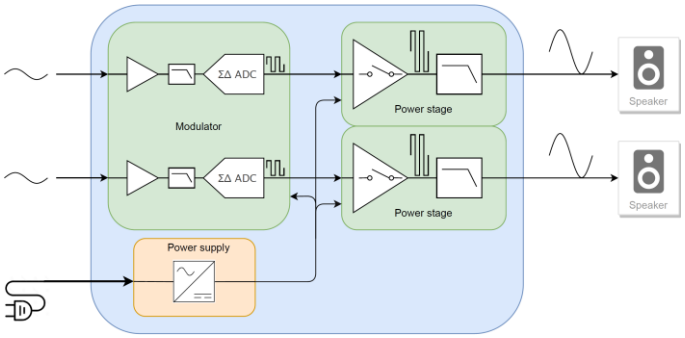

Fig. 5. General structure of the proposed amplifier

Before starting the design, the visible above structure of the device (Fig. 5.) was determined, and the following assumptions were made:

- use of a ready-made power supply with one output voltage of 24V,
- easy replacement of the modulated signal source,
- no global negative feedback loop,
- power stage made in the form of two mono modules with bridge-tied load (BTL) configuration,
- use of a ready-made, one-bit ΔΣ modulator intended for acoustic applications,
- the amplifier should operate with oversampling ratio of 128,
- load resistance of 4Ω.

Expected theoretical output power for given power supply voltage and load resistance was $72W_{RMS}$.

The ΔΣ modulator module would receive analogue signal, the level of which may reach +22dBu, with XLR inputs. Then, after attenuation and lowpass filtering the analogue signal would be modulated and transmitted to the output module.

The output module would receive the modulated signal and drive the switching block accordingly to the momentary state of the modulated signal. Finally, the high-frequency component would be removed with the LC-type lowpass filter before delivering the amplified signal to the speakers.

IV. ΣΔ Modulator Implementation

Since the design of a ΣΔ modulator is beyond the scope of this project, the PCM4202 ADC chip from Texas Instruments was chosen as a source of the modulated signal. Figure 6 shows internal structure [2] of this integrated circuit.

The PCM4202 ADC chip can provide on its output port signal coming directly from the internal one-bit modulator [2], with oversampling ratio that can be selected from 64 to 128. Furthermore, this chip does not require any microcontroller for configuration, which makes it perfect for this project.

The input buffer that is required to attenuate the analogue signal and to limit its bandwidth was implemented using the OPA1632 operational amplifier as proposed in the PCM4202s datasheet. The input buffer's gain was reduced to match the desired input signal level. Characteristics of this stage are shown in Fig. 7.

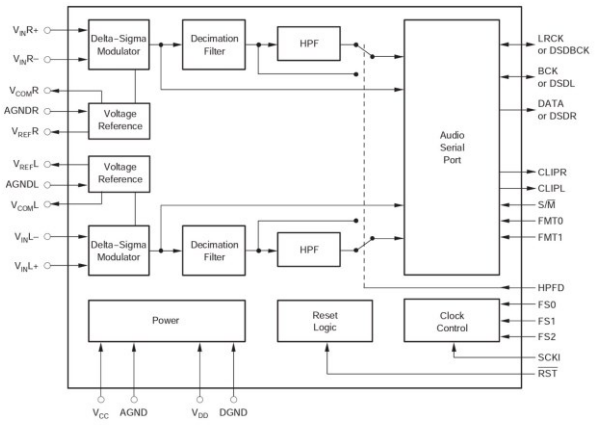

Fig. 6. Internal structure of the PCM4202 ADC chip

The red plot (Fig. 7.) shows the original characteristics of the input filter, while the blue plot was drawn after the gain adjustment. The 3dB bandwidth of the input filter is in both

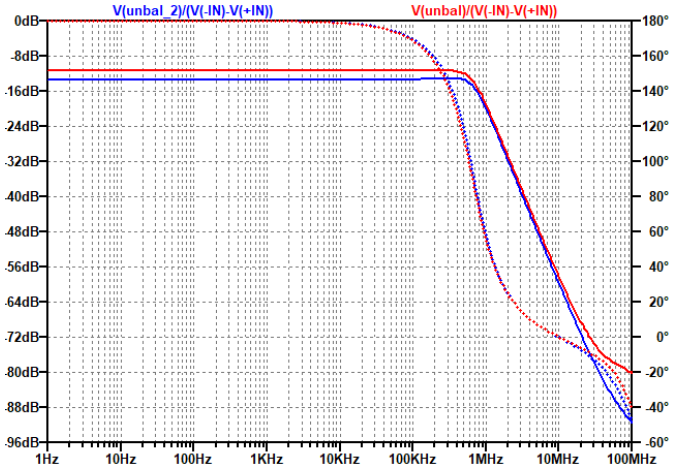

Fig. 7. Characteristics of the input filter

cases in range from 0Hz up to about 700kHz.

The assembled module is shown in Figure 8. On the left side of the module the XLR inputs are located, followed by the input buffers. The PCM4202 chip, along with the master clock generator are placed in the centre of the PCB. On the upper-right side of the module are the two output IDC connectors, while the lower-right side is occupied by the power supply section, consisting of several voltage regulators (separate for analogue and digital domain) and the power input.

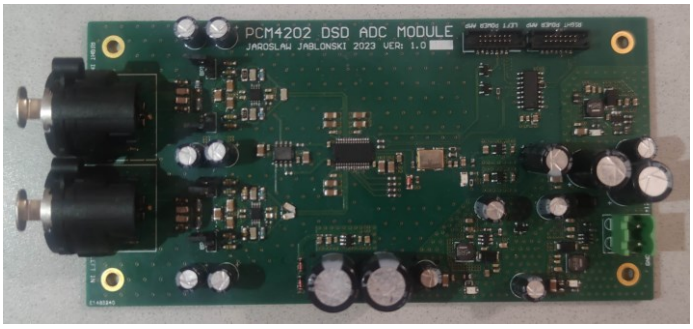

Fig.8. Assembled ΣΔ modulator module

V. Amplifier Implementation

The amplifier module consists of three main blocks: H-bridge driver, switching transistors forming the H-bridge and the LC-type lowpass filter.

As the H-bridge driver 2EDF7235K chips from Infineon [4] were used. These integrated circuits have two fully insulated output sections and a built-in dead time [3] controller. Internal structure and exemplary application are shown below in Fig. 9.

The 2EDF7235K chips offer up to 4A/8A (source/sink) driving current and can be used with maximal switching frequency of 10MHz [4].

The H-bridge was made of four N-channel MOSFETs PXN010-30QL. Basic parameters [5] of these transistors are listed in the Table I.

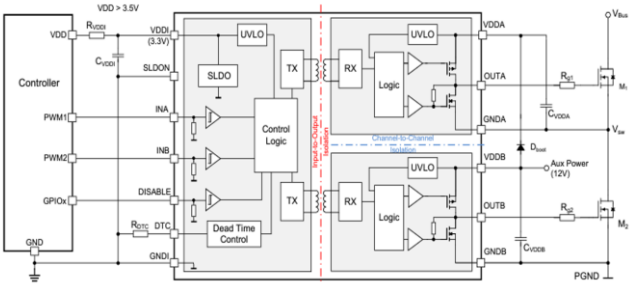

Fig.9. Internal structure and proposed application of the 2EDF7235K chip

TABLE I
BASIC PARAMETERS OF THE PXN010-30LQ TRANSISTOR

Name	Value
V_{DSmax}	30V
I_{Dmax}	6,5A
R_{DSon}	11,6mΩ
C_{ISS}	560pF
Package	MLPAK33 (3,3mm x 3,3mm)

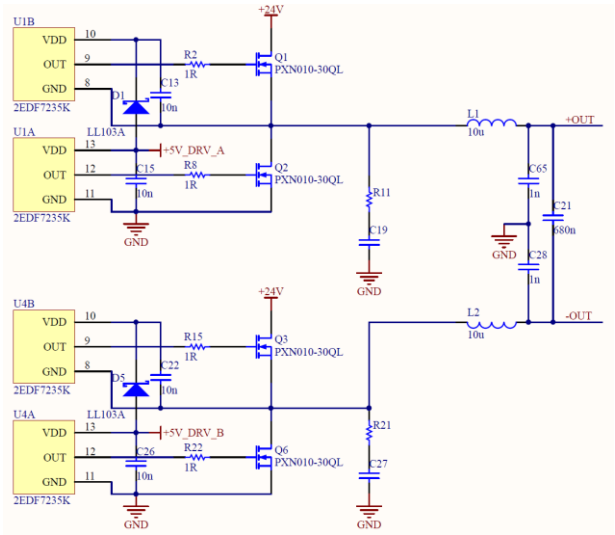

Fig.10. Full output stage of the amplifier

Figure 10 shows the schematic of the amplifier's output stage, including the LC lowpass filter.

The LC lowpass filter is Butterworth-type [6] with cutoff frequency tuned to 45kHz. Basic characteristics of this filter are shown in Fig. 11.

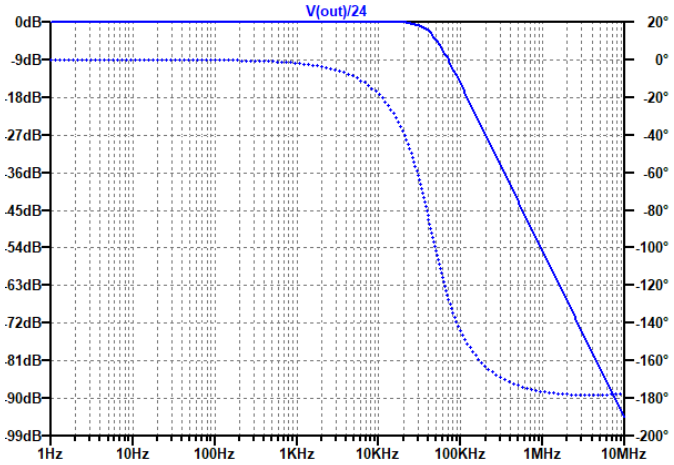

Fig.11. Characteristics of the LC output filter

As can be seen above (Fig. 11), the frequency response is flat up to 20kHz, however the phase shift of -40 degrees is introduced at this frequency.

Chosen transistors and driver chips, due to their small dimensions and optimised pinout, helped achieving good PCB layout (Fig. 12.), which is crucial in high speed and high current circuits.

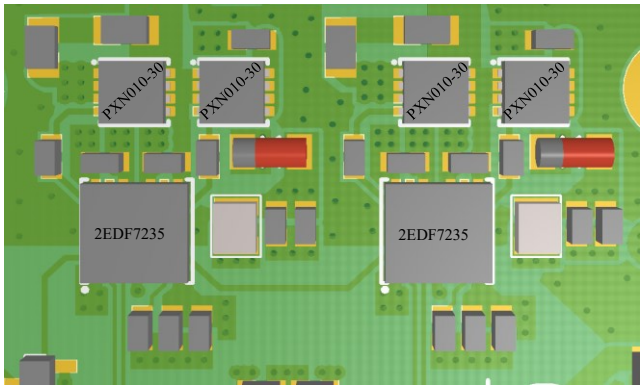

Fig.12. View of the switching transistors and their drivers (excerpt from the PCB layout design)

Figure 13 shows one of the assembled amplifier modules, while whole device can be seen in Fig. 14.

The amplifier module is much more densely populated, compared to the modulator module. Whole of the upper side of the module is occupied by power supply section, with voltage regulators and the power input connector on the right. The lower side of the module is divided into several sections that follow the signal flow. On the right the input IDC connector is located, followed by the control logic and signal conditioning circuits. Further to the left the drivers and the switching transistors are placed. Then, the LC lowpass filter is placed, followed by the

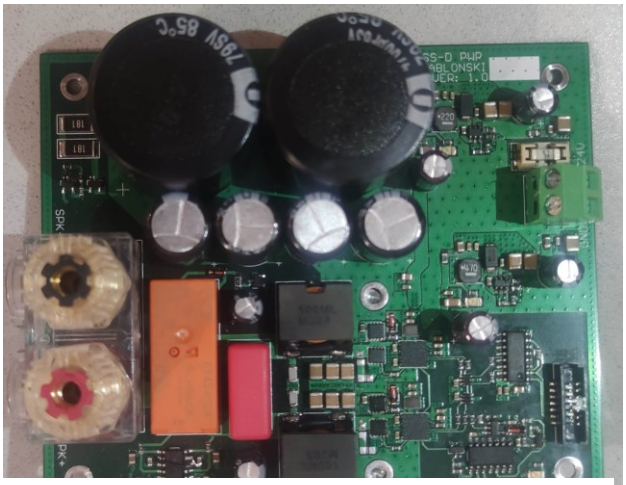

Fig.13. Assembled amplifier module

output relay and speaker connector. The output relay is driven by the DC protection circuit that is located below it.

Whole device consists of two such modules, visible in the middle of fully assembled amplifier (Fig. 14.), the ΣΔ modulator module (on the right) and the 24V 150W switching-mode power supply (on the left). A 12V voltage regulator was added to drop the voltage supplied to the modulator module. Modulated signals are distributed using 0,65mm-pitched ribbon cable.

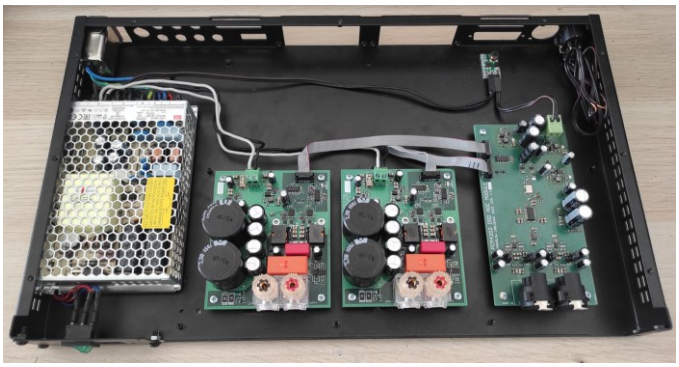

Fig.14. Fully assembled amplifier

VI. First Launch

When launching a new design for the first time, it is a good practice to perform it in several steps to minimize the risk of extensive damage. All the implemented circuits were divided into three categories:

- power supply and regulation,
- control logic and signal transmission,
- executive elements.

Several simple errors were found during first run of the modules. In the ΣΔ modulator module two electrolytic capacitors had reversed polarity. Also, polarity of one of the digital outputs was inverted. In the amplifier module reference voltages were swapped in the DC protection circuit.

All these errors were fixed in the manufactured modules without need to redesign them.

VII. MEASUREMENTS

Measurements were conducted using high quality DAC and ADC devices that were synchronised and connected to the computer. Room EQ Wizard software was used for data analysis with sine wave signal of 1kHz supplied to the amplifier's input. Figure 15 shows the setup described above, while FFT output spectrum with 1kHz sinusoidal input can be seen in Fig. 16.

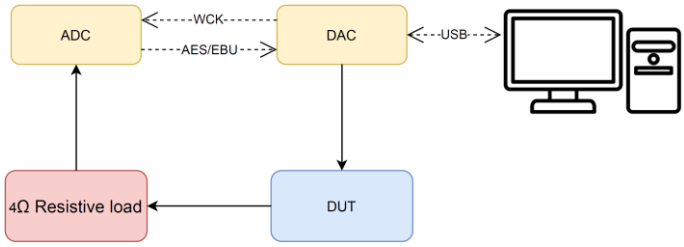

Fig.15. Equipment used for the measurements

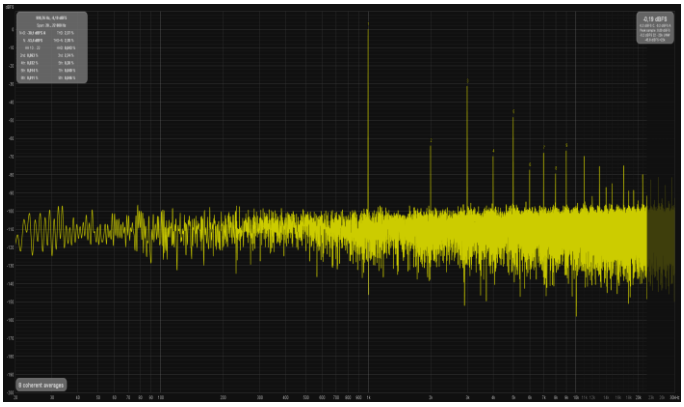

Fig.16. Spectrum of the output signal at $15W_{RMS}$

The highest spike seen in Fig. 16 is the fundamental frequency (1kHz), followed by both even and odd-order harmonics.

The measurements showed poor performance of the amplifier in terms of harmonic distortion and noise which could be related to insufficiency of the chosen modulator implementation. It turned out that the PCM4202 chip allows for achieving only up to 50% of modulation factor value for given maximal input signal level. This means that maximal output power of the amplifier is limited to ¼ of the value expected for the assumed power supply and load conditions. Table II presents results of conducted measurements.

TABLE II
RESULTS OF THE MEASUREMENTS

Parameter	Value
THD	2,72%
THD+N	2,73%
Dynamic Range	66,2dB
Out. Power at THD = 1%	$3,8W_{RMS}$

To test the output stage at maximal designed output power and to measure amplifier's efficiency, input signal level was further increased until the modulator became unstable. Although the risk of damaging the PCM4202 chip was high, the experiment was successful and allowed to determine the amplifier's parameters listed in the Table III.

TABLE III
OUTPUT POWER AND EFFICIENCY

Parameter	Value
Theoretical max. output power	$72W_{RMS}$
Measured max. output power	$61W_{RMS}$
Measured efficiency	90,5%

VIII. CONCLUSION

This paper presents the circuit design and measurement results of a modular class-D audio amplifier. System is designed to allow easy replacement of modules to further improve the performance.

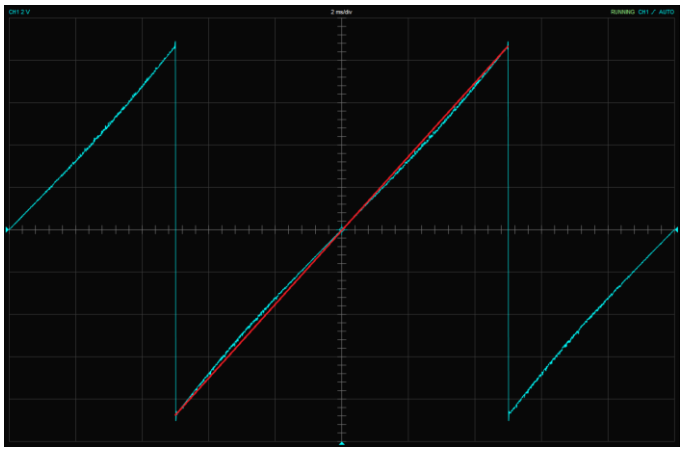

Fig.17. Nonlinearity of the designed amplifier

The results of the measurements revealed several properties of the modulators that must necessarily be optimized for use in audio systems. The so-called dead time, which introduces errors to the D/A conversion at the output can degrade THD+N ratio. These errors could be significant when the signal level is low because this is when the ΔΣ modulators change their output's state most frequently [1]. Figure 17 shows the actual nonlinearity of the designed amplifier.

Fig.18. Transistor gate driving signals and their dead time

Minimal duration of the dead time that can be configured in the 2EDF7235K driver is 15ns [4], which is quite significant, relative to one bit duration of 345,3ns (Fig. 18).

The implementation of the specific ΔΣ modulator with limited modulation depth at 50% is not sufficient to achieve satisfactory performance in terms of output power.

The completed amplifier achieves its goal to serve as a foundation for future work and development of switching-mode acoustic amplifiers because it can be easily modified in several ways, which may help resolving revealed issues. The oversampling ratio can be reduced from 128 to 64 to decrease impact of the dead time on overall performance. As a side effect, the efficiency should also improve. A global negative feedback loop potentially can be added, but care must be taken to keep the amplifier from oscillation.

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