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New Synchronization Method for Transmission Systems with Variable Length of Bits

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***Abstract*—Based on the Spartan 3E evaluation module, a flexible platform for the implementation of different algorithms for A/D conversion was developed. The aim of presented work was to improve the concept of the sampling rate adaptation to the input signal rate of change in terms of practical issues including synchronization of delta codecs. The new, original synchronization method, useful in systems dedicated for transmission of variable duration of bits was proposed and experimentally verified. Performed measures and observations have shown elimination of the synchronization lose phenomenon.**

***Keywords*—delta modulation, adaptation, non-uniform sampling, synchronization, codec**

I. Introduction

THE investigation aimed at the improvement of A/D conversion efficiency prove that not all potential possibilities of delta modulation are fully utilized, so far.

The compression properties of delta modulation systems are based on a rule that this conversion is accomplished on the removed redundancy of an input process. The efficient samples decorrelation is usually made using the adaptation procedures [1, 2]. The step size adaptation is the simplest one.

In 1-bit adaptive delta modulators (ADM) a wide dynamic range (*DR*) and high quality conversion (*SNR – signal to noise ratio*) are obtained due to the adaptation of the quantization step size or/and the sampling interval.

The long-term research works [1, 3, 4] allow to affirm, that reaching high accuracy and large noise immunity in wide dynamic range, with use of the uniform sampling ADM converters, is not possible. Therefore is proposed to use the 2 - parameters, 1-bit delta modulation, in which both the step size and sampling interval are adapted. The results of simulating works proved that for non-stationary sources, the adaptive sampling delta converters expose higher coding efficiency than the previous proposals, based on uniform sampling methods.

The aim of presented work was to develop the concept of the sampling rate adaptation to the input signal rate of change in terms of practical issues including synchronization of delta codecs [5]. Two evaluation modules (Spartan 3E) [6] have been used to build a flexible platform with the ability to implement different delta codec's algorithms and making studies of synchronization method for delta codecs with non-uniform sampling rate.

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This paper addresses the problem of synchronizing clocks in the transmission systems, including the non-uniform sampling codecs.

In one of the best known methods of synchronization, the clock signal embedded into the transmitted bit stream and next extracted by the receiver. An alternative method to encoding the clock in the transmitted bit stream is to apply a constant clock source at the receiver which is kept in time synchronism with the incoming data bits. In this technique it is required to encode the data in such a way that there are all the time enough bit transitions in the transmitted waveform to permit the receiver clock to be resynchronized at frequent intervals. Usually classical digital phase-locked loop (DPLL) is used to maintain bit synchronism in systems with constant clocks. DPLL to proper work needs only a very small correcting at irregular intervals. Hence, to take advantage of DPLL a main clock source (crystal-controlled oscillator), should hold its frequency sufficiently stable.

In the article the method of synchronization employing a temporary adding of single main clock period has been applied in decoder.

II. ANS-DM Modulation

Several military and commercial systems use delta modulations with uniform and non-uniform sampling. Many semiconductor vendors produce specialized IC's based on delta system (pacemakers, CAT scans, MRI scan). The very spectacular application of delta technique has been voice encoding system used in the Shuttle system. It has been chosen by NASA because of its tolerance to channel errors [2, 4].

ANS-DM (***A**daptive **N**on-uniform **S**ampling - **D**elta **M**odulation* [3]) codecs, are 1-bit delta converters with step size and sampling instant adaptation. **NS-DM** (***N**on-uniform **S**ampling - **D**elta **M**odulation* [3]) codecs, are 1-bit delta converters with sampling instant adaptation only. For this method step size is fixed.

Adaptation of two parameters (ANS-DM) makes the hardware implementation of the delta coder more complicated in relation to the solutions with one parameter adaptation (NS-DM), but increases the quality of conversion (*SNR*). The total dynamic range (*DR*) of the delta converters with two parameters adaptation is a product of the each parameter companding gain [2, 3].

For the input signal $x(t)$ the predicted signal $s(t_j)$ at time t_j (Fig.1) is given by expression (1):

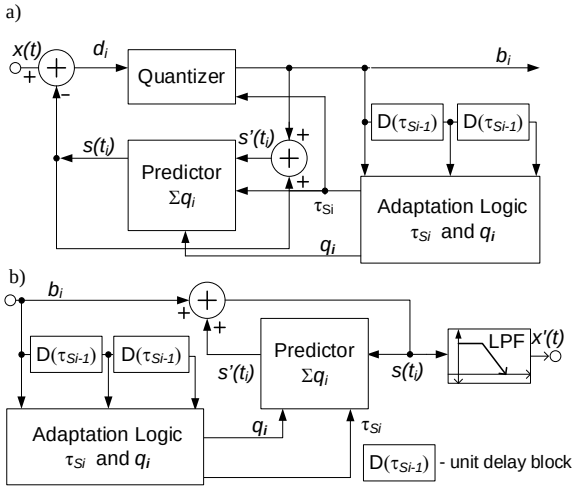

Fig. 1. Block diagram of ANS-DM codec: a) coder, b) decoder.

$$s(t_j) = s(t_0) + \sum_{i=0}^{j-1} d_i q_i \ , \tag{1}$$

where: $d_i=sgn[x(t_i)-s(t_i)]$, and: q_i – *i-th* quantization step size.

The output code stream is:

$$b_i = \begin{cases} 1 & for \quad d_i = 1 \\ 0 & for \quad d_i = -1 \end{cases} , \tag{2}$$

where: b_i –digital value of the output bit.

Let τ_s be the sampling interval. The sampling interval $\tau_s = t_{i+1} - t_i$ vary according to the characteristics of $x(t)$ thus the next sampling time t_{i+1} is expressed as:

$$t_{i+1} = t_i + \tau_s \tag{3}$$

Value of the sampling interval τ_{si} is determined by the algorithm:

$$\tau_s = \begin{cases} K1 \cdot \tau_{s-1} & for \quad b_i = b_{i-1} = b_{i-2} \\ K2 \cdot \tau_{s-1} & for \quad b_i \neq b_{i-1} \neq b_{i-2} \\ \tau_{s0} & other \ cases \end{cases} , \tag{4}$$

where: $K1$, $K2$ are constant factors of interval time modification and $K1<1<K2$. For audio signals usually $K1$=0,6÷0,9, $K2$=1,1÷1,4 are used.

Generally, in ANS-DM modulation algorithm, the limitation of the maximum and minimum sampling interval values are:

$$\tau_s = \tau_{s\max} \ if \ K2\tau_s > \tau_{s\max} \ and \ \tau_s = \tau_{s\min} \ if \ K1\tau_s < \tau_{s\min} \ , \tag{5}$$

τ_s - start sampling interval and this value decides about the average output bit rate and $\tau_{smin} < \tau_{s0} < \tau_{smax}$.

Quantization step size q_i adaptation is determined by the algorithm [3]:

$$q_i = \begin{cases} q_{i-1} \cdot P & for \quad b_i = b_{i-1} = b_{i-2} \\ q_0 & other \ cases \end{cases} , \tag{6}$$

where: P is constant factor of the step-size modification with $1 < P$. For audio signals usually P=1,2÷2,0 are used.

Generally in ANS-DM coder algorithm the limitation of the maximum and minimum step-size values are:

$$q_i = q_{i\max} \ if \ Pq_i > q_{i\max} \ and \ q_0 = q_{\min} \ . \tag{7}$$

Formulas (4) and (5) represent the 3-bit adaptation algorithms of the change of the sampling interval. One can see that the ANS-DM output binary stream carries the information about the sampling interval and the step values allowing reconstruction of the input signal. So that in the decoding process the irregular staircase signal can be recovered. ANS-DM encoder output stream carries the information about sampling instant and step size values [2, 3]. The mechanism of return of sampling instant and step size to τ_{s0} and to q_0 (4), (5) in the ANS-DM coder increases the tolerance to channel errors and provides to the synchronization when decoder is turned on.

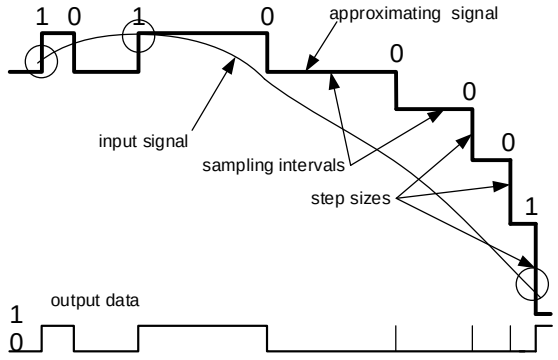

Fig. 2. Timings of the ANS-DM modulation.

ANS-DM modulation bases on the (4) and (6) functions which modifies the sampling interval and the step size according to the time-varying slope characteristics of the input signal. In this way an ANS-DM approximation staircase waveforms (Fig. 2) are better fitted to the source signals than others delta modulations (LDM, NS-DM).

III. Description of Codecs Implemented in the Spartan Evaluation Module

The universal delta codec implemented using the Spartan 3E evaluation module [6] was used for tests. At the encoder input an amplifier with software adjustable gain is placed (Fig. 3). Its output is connected to the A/D converter, which generates (with the base clock cycle $1/f_b$ = 720 ns) 14 bit representation of the instantaneous value of the analog input signal.

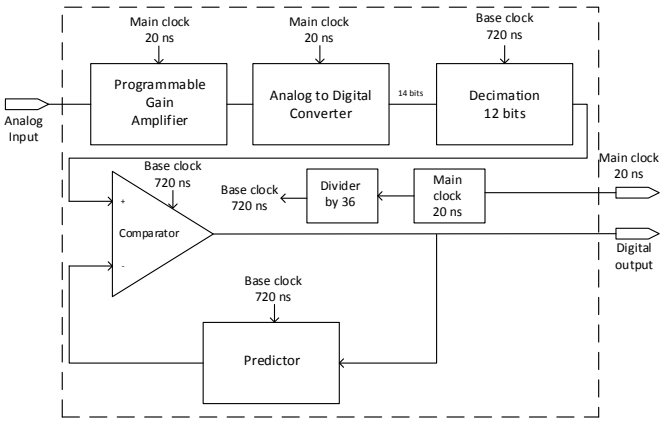

Fig. 3. Block diagram of an encoder built on the base of Spartan evaluation module.

After decimation the representation is reduced to 12 bits (due to the resolution of the D/A decoder) and that value is compared with the value at the output of the predictor (Fig. 3). Depending on which signal is greater, the output of the encoder produces logical zero or one. LDM, NS-DM, ANS–

DM encoding methods, differ mainly only in the construction of the predictor. Base clock and controlling digital modules (decimator, comparator and predictor) is derived from the main clock (f_m = 50 MHz).

Decoder (Fig. 4) contains a predictor and 12-bit D/A converter. On the basis of the subsequent one-bit digital values from the encoder output, predictor generates consecutive 12-bit words, approximating the instantaneous values of the input signal. These words are given to the input of the D/A and consequently generate on its output staircase signal, approximating the signal at the encoder input. Similarly to the operation in the encoder, D/A converter is controlled by the main clock.

Just as in the encoder, operation of the predictor in the decoder module are controlled by the basic clock (720 ns) produced from the main clock. As the main clock of decoder, internal generator or external signal (eg. from the encoder) can be adopted (Fig. 4).

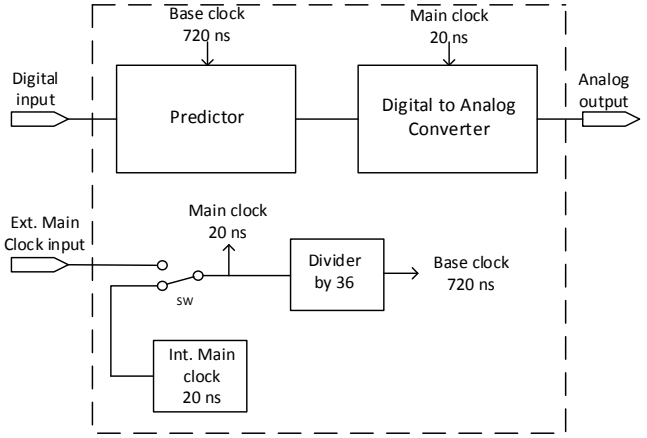

Fig. 4. Block diagram of a decoder implemented based on the Spartan evaluation module.

Universal delta codec developed using the Spartan 3E evaluation module enables implementation of various delta processing algorithms [2, 6]. In this, for example:

- NS-DM algorithm with parameters:

$K1$=0.77, $K2$=1.3; τ_{p0} =2.88µs; τ_{smax} = 56.88µs; τ_{smin}= 0.72µs; q=q_0=U_{ref}/128 = 19.54 mV for U_{ref} = 2.5 V.

- ANS-DM algorithm with parameters:

$K1$=0.77, $K2$=1.3; τ_{s0} = 6.48µs; τ_{smax}=33.84µs; τ_{smin}=0.72µs; P =1.5; q_0= 4.88mV, q_{max}=37.23mV.

All implemented algorithms work properly and allow reconstructing the analog input signal with *SNR* ratio above 20dB.

IV. CLOCK SYNCHRONIZATION SYSTEMS

Synchronization is an act of coordination processes in time. In practice, it should lead to the compatibility of two or more periodic phenomena. In case of a data transmission [5, 7] synchronization means delivering and tracking (or only tracking) of the clock signal in the receiver in the comparison to the information contained in the received signal.

In the discrete phase locked loop (DPLL) with a local oscillator whose frequency is reduced N times, to achieve synchronization a required frequency changes are obtained by varying coefficient of oscillator divider (o.e. N-2, N-1, N, N+1, N+2). Fig. 5 presents block diagram of this DPLL.

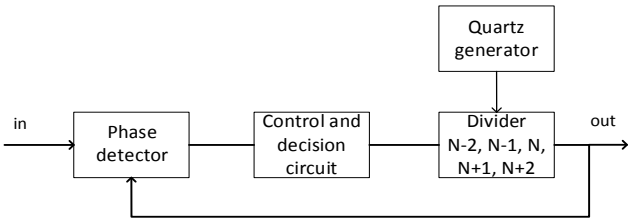

Fig. 5. Block diagram of a digital PLL using discrete divider instead of linear VCO.

Usually classical digital phase-locked loop (DPLL) is used to maintain bit synchronism in systems with constant and variable clocks. DPLL to proper work needs only small correcting at irregular intervals. To take advantage of a DPLL, the frequency of main clock source should be enough stable. The frequency of the main clock source is N times higher than the bit rate employed on the data link and this in sequence is used by the DPLL to determine the time intervals between successive samples of the received bit stream. Thus, assuming that the decoder input bit stream and the local base clock are in synchronism, the state of an input bit signal is sampled at its center with exactly N clock periods between each sample (Fig. 6a) [8].

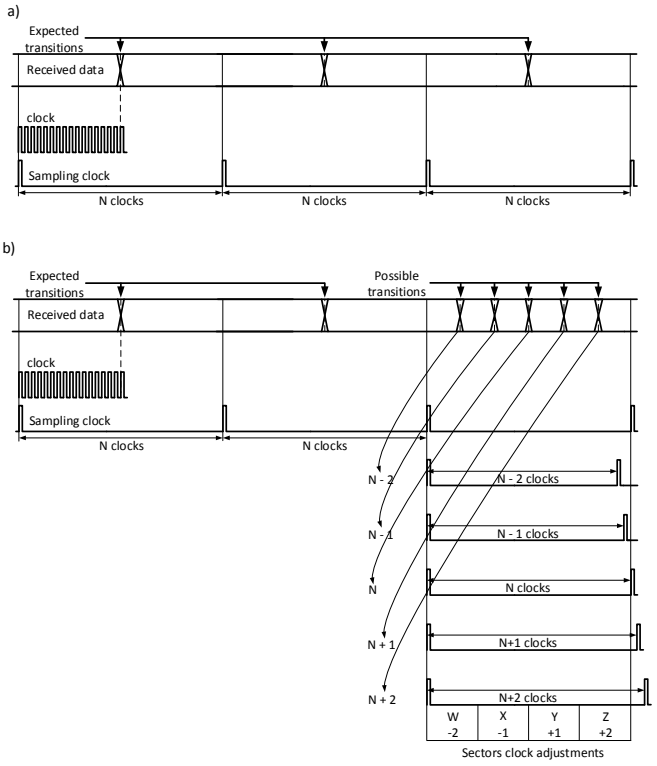

Fig.6. Digital PLL operation: (a) during synchronization; (b) clock adjustment rules [8].

Problem occurs when the incoming bit stream and local base clock drift out of synchronism. Then the fitting of the sampling instant is carried out in discrete way as shown in Fig. 6b. If there are no transitions on the decoder input, the DPLL simply set up a sampling pulse every N clock periods

after the past one. At any time a transition is noticed, then, the time interval between the past set up sampling pulse and the next one is determined according to the position of the transition in regard to where it should occur. To obtain this, each bit period is divided e.g. into four quadrants, shown as W, X, Y and Z (Fig. 6b). Each quadrant is equal to N/4 clock periods and if, e.g., a transition appears during quadrant W, this denotes that the last sample was in fact too close. The time period to the next sample is in consequence cut to 30 clock periods. Alike, if a transition occurs in quadrant Z, this denotes that the past sample was too far. The time period to the next sample have to be expanded to 34 clock periods. Transitions in quadrants X and Y are closer to the expected transition and thus the relative fitting are less (31 or 33 clock periods, respectively). Hence, subsequent corrections set up sampling pulses close to the center of each bit period [8].

V. Transmission Without Clock Recovering Mechanism

In order to eliminate the hazards during signal reconstruction in decoder, usually a single D-type flip-flop at the output and two D-type flip-flops at the input of the encoder are used (they are clocked with the main clock). Since the input and output buffers of the Xilinx XC3S500E fulfill the role of D flip-flops on the input and output, so only the decoder uses an additional D-type flip-flop (Fig. 7).

Applying the unsynchronized local clocks in the coder and decoder, due to differences of frequency values, causes a typical phenomenon of phase shifting between these clocks.

After a specified period of time, the phase shift leads to short synchronization lost.

In this work the source of the main clock, was crystal oscillator FCO-736B-50,000 with an accuracy of ± 2500Hz (± 50 ppm) [6].

However, the relative differences between frequency of crystal generators used in the coder and decoder are most important. Generally one of the generators, at the same ambient conditions, has a slightly higher frequency than the second one and this difference is approximately constant.

Solutions of synchronization based on unsynchronized local clocks (Fig. 7) as expected, causes regular synchronization fails. Its influence to output waveforms was shown in Fig. 8.

The synchronization fails occurs when the phase shift is so high that the data reading takes place at the time of the slope duration. This leads to a considerable distortion in the decoder output. After some time, the reading point again occurs in the areas where the signal has the certain logical zero or one level, and synchronization comebacks.

Measured value of the interval between synchronization fails in ANS-DM test system (based on FPGA circuit – Spartan 3E with crystal oscillator) was slightly greater than 0.35 sec.

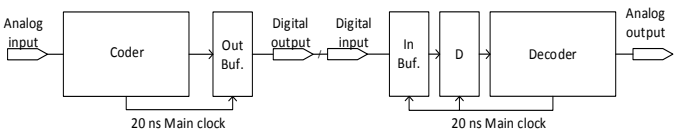

Fig. 7. Block diagram of the transmission system codec with local unsynchronized clocks.

Simple calculations, confirm that the cancelation of synchronization fails are consequence of the generators frequency differences. If the error of the main clock (f_m) is denoted by Δ, then a time error on one period of this clock is:

$$\Delta T_m = \frac{\Delta}{f_m(f_m+\Delta)} \quad . \tag{8}$$

The time at which the consecutive synchronization fails is given by:

$$T_\Delta = \frac{n}{\Delta} + \frac{n}{f_m} \quad . \tag{9}$$

where $f_b/f_m=n$. For n=36, f_m = 50 MHz and Δ=96 Hz the T_Δ=0.375sec, so it is similar to the value obtained experimentally.

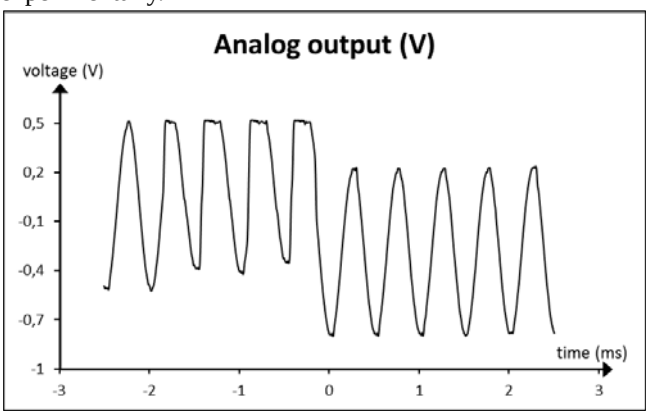

Fig. 8. The effect of the synchronization lose observed in the decoder output signal, that works with local clocks as in Fig. 4 (for sinusoidal signal).

Summing presented till now effects, it is true that in the system with unsynchronized local clocks the amount of disruption at the decoder output (Fig. 6) caused by the temporary synchronization lose depends on the clocks frequency difference in coder and decoder, and its time duration is influenced by the slope steepness of a data stream. In the case described in article duration of disturbance caused by the cancellation of synchronization was amounted to about 1.3 ms.

VI. New Synchronization Method Addressed to System With Variable Duration of Bits

To synchronize the coder-decoder system many approaches lead towards to use information comes from data signal on the decoder input and control a local main clock by this records (Fig. 9).

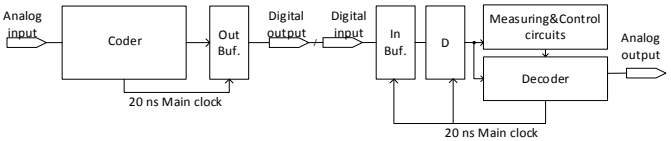

Fig. 9. Block diagram of codec transmission system with synchronization based on the data signal on the decoder input.

In the proposal synchronization method dividing coefficient (Fig. 10) is determined by dynamic parameters of A/D and D/A converters used in described codecs. Data processing

requires a total 35 main clock periods. This value is a consequence of serial transmission synchronization. For practical reasons to implement decoder it had been taken 36 main clock periods.

Since synchronization processes depends mainly on the main clocks frequency difference, the use of DPLL shown in Fig. 5 would require a local oscillator with a frequency many times higher than the frequency of the main clock. Therefore, there was decided to use for the synchronization a techniques of temporary decreasing the number of main clock pulses in decoder. Base clock pulses are used for the measurement of the main clocks frequency deviation between transmitter and receiver. If the maximum clock frequency in the D/A converter is used, this method is applicable only when main clock frequency in receiver (decoder) is higher than the main clock frequency of the transmitter (coder). A block diagram of synchronization procedures in the decoder is shown in Fig. 10.

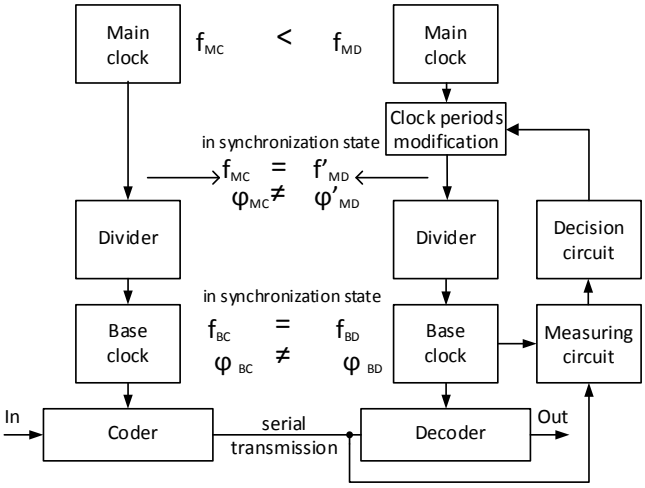

Fig. 10. Synchronization procedures in transmission systems with variable duration of bits.

The idea of the used technique based on the temporary extension a low state of the main clock signal (by one period) resulted in reduction of the number of main clock edges is shown in Figure 11b.

In described transmission systems too high phase shift causes breaking of the synchronization. To protect the transmission system against the synchronization breakdown the method employing temporary decreasing number of the main clock pulses (adding of single main clock period) has been applied in decoder. Measuring and control circuits (Fig. 9, 10) are implemented for this purpose.

The previously described parameters of main generators and codecs allows keeping synchronization by adding one of main clock period to equal the temporary difference between period of main clock in coder and decoder. The added period of clock is inserted in this part of the base clock waveform, which does not affect the work of the predictor and D/A converter (Fig. 8).

Experimental studies have shown elimination of the synchronization lose phenomenon, which are typical in system of encoder and decoder with the local unsynchronized clocks.

An opposite approach is also possible, if the main clock in the encoder is slightly slower than in the decoder. A method based on temporary increasing the number of main clock pulses can be applied in decoder. However, this solution takes a great risk of disturbing predictor and D/A converter work. Moreover this method could be applied only when the frequency of main clock is lower than the maximum operating frequency of A/D and D/A converters (Fig. 11). Current analyses are focused on discovering an implementation of synchronizing mechanism, working irrespective of the sign of the difference between the clocks frequency in the coder and decoder.

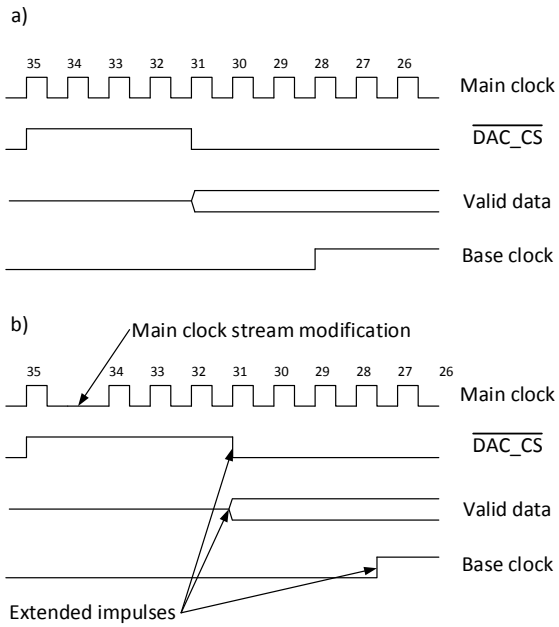

Fig. 11. Synchronization processing: a) during synchronization, b) main clock stream modification causes extending all produced signals.

VII. Conclusions

This paper addresses the problem of synchronizing clocks in the transmission systems, including the non-uniform sampling codecs.

The article presents the original application of evaluation modules Spartan 3E used to study of the synchronization procedures in transmission systems with variable duration of bits. A flexible platform for implementations different algorithms of delta codecs with step size and sampling interval adaptation (NS-DM and ANS-DM) was designed. The experiments have confirmed the correct functioning of ANS-DM and NS-DM codec hardware implementation.

The use of local unsynchronized clocks (in the coder and the decoder) and transmission without clock recovering mechanism obviously leads to synchronization loses and distortions in an analogue reconstructed signal. To minimize these effects an additional procedures of the clock synchronization are required.

Conception of the classical digital phase-locked loop used to maintain bit synchronism in transmission systems has been shown. In this idea a main clock can hold its frequency sufficiently constant. DPLL to proper work requires only small correction during irregular intervals.

The synchronization mechanism with temporary decreasing of the main clock edge numbers in decoder has been proposed. It provides the correct synchronization of the bit stream

transmission with a variable time base. Suggested method assumed that the absolute value of the clock frequency in the coder is lower than in the decoder. Currently, the implementation of synchronization procedures with both decreasing and increasing the main clock pulses in receiver has been investigated.

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