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Identification of Circuit Parameters for the Specified or Measured Performances

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***Abstract*—Extension of the method of analog circuit parameter identification for the specified design performances, originally presented by the same author in 1982, is described. These parameters are designated by means of PSpice simulation of the adjoint circuit to the original one. In this adjoint circuit, elements of the original circuit, described by the sized parameters, are replaced by controlled sources. Each such source is controlled by the differential voltage or current, difference between the calculated voltage or current and the specified one, with infinitely large gain. The method is applicable to both linear and nonlinear DC circuits and AC circuits and can be used in many fields of analog circuit design, such as: finding of acceptability region, analog fault diagnosis, postproduction identification and tuning. In the later cases, design performances are replaced by measurements of Circuit Under Test (CUT). Simplicity, extremely low computational complexity and high accuracy are the main benefits of the proposed, basic Circuit Theory based, approach – the solution is found after a single PSpice simulation. For better understanding of the presented methodology, five practical examples are discussed.**

***Keywords*—analog circuits, parameter identification, fault diagnosis**

I. Introduction and Problem Statement

THE problem of sizing selected circuit parameters for the specified or measured design variables, performance characteristics, is one of the fundamental problems in analog circuit design and fault diagnosis. Assume that a circuit has its performance characteristics, set by the design engineer or measured, such as:

- Voltage, DC voltage U or AC voltage phasor $U(j\omega)=U(\omega)\exp[j\alpha_u(\omega)]$ (1)
- Current, DC current I or AC current phasor $I(j\omega)=I(\omega)\exp[j\alpha_i(\omega)]$
- Power, DC power P or AC real power $P(\omega)=I(\omega)U(\omega)\cos[\alpha_u(\omega)-\alpha_i(\omega)]$
- Gain, DC gain U_{out}/U_{in} or AC gain $U_{out}(\omega)/U_{in}(\omega)$ and phase shift $\alpha_{out}(\omega)-\alpha_{in}(\omega)$
- Input Resistance (Impedance), DC input resistance $R_{in}=U_{in}/I_{in}$ or AC input impedance $Z_{in}(j\omega)=U_{in}(\omega)/I_{in}(j\omega)=R_{in}(\omega)+jX_{in}(\omega)$

The performances are given as N-vector (2):

$$\mathbf{F}=[F_1\cdots F_N] \tag{2}$$

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These performances, set by the design engineer or measured, are designated by circuit parameters: passive parameters, such as resistance R, capacitance C, inductance L, controlled source gain or coupling coefficient k and/or active parameters, such as supply voltage or current. Thus, circuit parameters are considered as M-vector (3):

$$\mathbf{X}=[X_1\cdots X_M] \tag{3}$$

Circuit topology relates circuit parameters (3) to circuit performances (2):

$$\mathbf{F}=[F_1\cdots F_N]=\mathbf{F}(\mathbf{X}) \tag{4}$$

Usually, circuit performances (2) are constrained by performance design specifications (5):

$$\mathbf{F}_{\min}\leq\mathbf{F}(\mathbf{X})\leq\mathbf{F}_{\max} \tag{5}$$

In analog circuit design, this region in performance space, called the feasible region, is mapped into the parameter space, to form the acceptability region and numerous methods of this mapping have been proposed [1-3]. Then, after design centering, nominal values of circuit parameters and their design tolerances are set, to create the so called tolerance region. The method described in [2], for voltage and current performances in DC circuit, called further on "adjoint circuit method", is based on analysis of the adjoint circuit with identified elements replaced by controlled sources with infinitely large gain. In this paper, the extension of this method on AC circuits and arbitrary performances (1) is presented, application of PSpice simulations is proposed.

In circuit design, normally $N\geq M$. To find coordinates of a single vertex of acceptability region a single combination of $N=M$ performances $\mathbf{F}^*=[F_1^*\cdots F_M^*]$ is selected, i.e. the number of sized parameters (3) is equal to the number of performances (2).

In parameter identification based approach to analog fault diagnosis, $N=M$ in a natural way (number of measurements = number of identified parameters).

In general case, the explicit formula that expresses M parameters by $N=M$ performances (6) is not available.

$$\mathbf{X}=[X_1\cdots X_M]=\mathbf{G}[F_1^*\cdots F_M^*] \tag{6}$$

This mapping can be easily designated by analysis of adjoint circuit, in which the sized (identified) parameters (elements) $\mathbf{X}$ are replaced by controlled sources, controlled by the specified or measured performances $\mathbf{F}^*$, as described in the next Section II for different performances (1). In 2014, R. Hashemian published the method of parameter identification, of finding the mapping described by (6) [4]. This method is based on

fixator-norator pairs (FNPs) concept [5] and its findings happen to be practically identical with findings of the adjoint circuit method, presented originally in 1982 [2] and extended in this paper. The only difference is in the method description, theoretical background, while the final circuit for PSpice simulation is practically identical for both methods. This similarity or rather identity is demonstrated in Section III, on a benchmark example.

II. Adjoint Circuit Method

The idea of using controlled sources to size parameters $\mathbf{X}=[X_1 \cdots X_M]$ for the specified design performances $\mathbf{F}^*=[F_1^* \cdots F_M^*]$ is presented in the block diagram of Fig. 1.

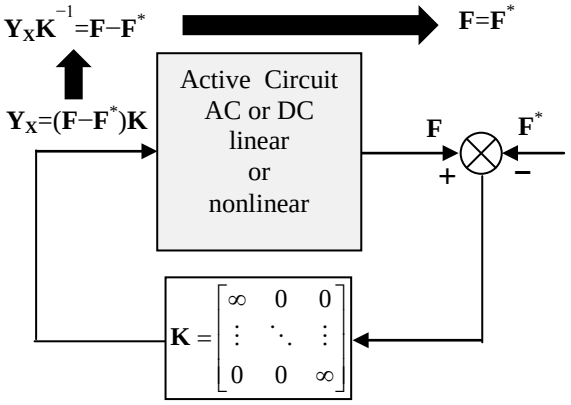


Fig. 1. The idea of using controlled sources to size parameters **X** for the specified performances $\mathbf{F}^*$; $\mathbf{Y_X}$ are controlled sources that replace elements characterized by **X**

To find the mapping (6), the adjoint circuit is created and analyzed, by means of PSpice. In this circuit, elements described by the sized parameters are replaced by controlled sources. Each such source is controlled by the differential voltage or current F_δ, difference between the calculated voltage or current F and the specified one F^*, with infinitely large gain k (practically k=10 Meg). To simplify and unify the circuit description only four diagram symbols are used, as depicted in Fig. 2:

a) resistor (linear or nonlinear), also real and imaginary part of impedance, arbitrary element, e.g. arbitrary independent source,
b) voltage source, DC or AC, independent or dependent,
c) current source, DC or AC, independent or dependent,
d) arbitrary controlled source,

a zero current/voltage source (o.c./s.c.) has no arrow inside.

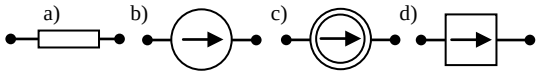


Fig. 2. Circuit symbols used in circuit diagrams

Use of controlled sources to size (identify) circuit parameters, for the given, specified or measured, circuit performances is presented in Fig. 3. The original circuit is presented in Fig. 3a, the adjoint circuit for the given current I^* or voltage U^* is presented in Fig. 3b, for power P^* in Fig. 3c, for gain K^* and input resistance R_{in}^* in Fig. 3d. PSpice notations of controlled sources are used – CCCS is denoted by F, same as generalized design performance!

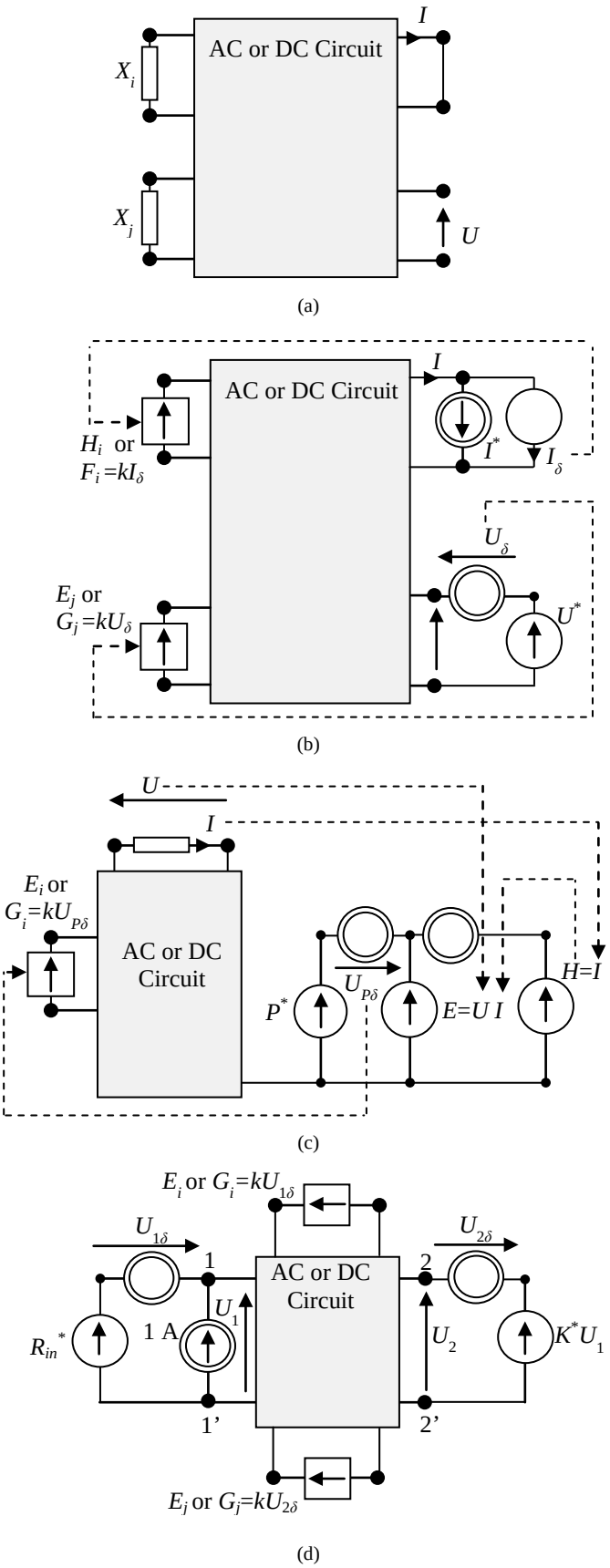


Fig. 3. Original circuit a) and adjoint circuits for the specified b) current I^* and/or voltage U^*, c) power P^*, d) gain K^* and input resistance R_{in}^*

The character of the controlled source that replaces the sized element (parameter): CCVS H or CCCS F (same notation as for performance is used) for current I_δ and VCVS E or VCCS G for voltage U_δ, is arbitrary. Also, assignment of the controlled source to the specified performance is arbitrary.

The circuits of Fig. 3 are DC circuits and circuit variables are real numbers. For AC circuits, these variables have to be replaced by complex numbers (1). Methodology of creating the adjoint circuits of Fig. 3, the way of replacement of the sized element (parameter) by the controlled source and designation of controlling voltage or current, for different performances (1) is explained on exemplary circuits.

III. Adjoint Circuit Method Versus FNPs Method

Consider the circuit in Fig. 4a [4]. The transimpedance $R^*=U_o^*/I_1$=10 kΩ is expected, while $X=R_3$ is the identified parameter.

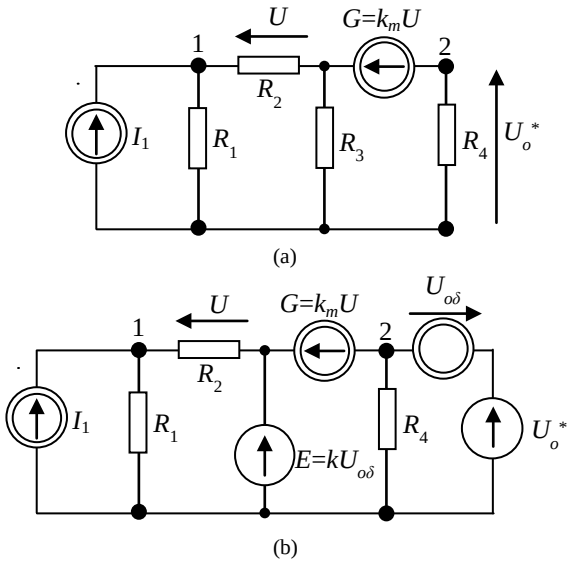


Fig. 4. Exemplary circuit [4]: a) original, b) adjoint

For the assumed I_1=1 mA, the specified performance is $F^*=U_o^*$=10 V. Other circuit parameters are as follows: $R_1=R_4$=2 kΩ, R_2=1 kΩ, k_m=9 mA/V. When using the FNPs method, a fixator U_o(10 V,0) is assigned to the output port and R_3 is replaced by a norator R_3(−,−). Then, the norator is replaced by a VCVS with very high (10 Meg) gain and the fixator with a voltage source U_o=10 V in series with arbitrary resistance. This circuit is practically identical as the circuit depicted in Fig. 4b, obtained from the adjoint circuit method, originally described in 1982 [2]. The only difference is in character of element added to produce the controlling voltage: arbitrary resistance in FNPs method [4], zero current source in adjoint circuit method [2]. The character of this element is meaningless for the intended simulation and this is practically the only original finding of the FNPs method if compared with the adjoint circuit method. The methods differ in description indeed but the final effect, a circuit for PSpice simulation, is practically the same.

IV. Exemplary Circuits

Five exemplary circuits are discussed. For some of them the explicit formula (6) can be found algebraically, by means of simple circuit analysis. In such case, use of CAD is not necessary. It has to be emphasized that the primary task of all presented examples is to show the methodology, using the introduced adjoint circuit concept, for different configurations of parameters and performances.

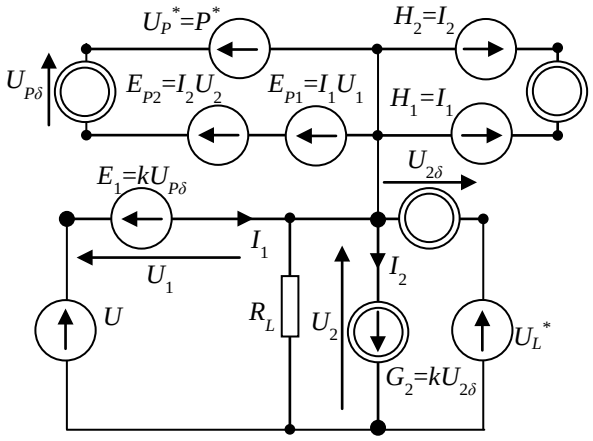
A. Voltage Divider

For the voltage divider built of resistors R_1 and R_2, supplied from U=12 V input voltage and loaded by R_L=1 kΩ (in parallel with R_2), the task is to size the resistances R_1 and R_2 such that $U_2^*=U_L^*$=10 V and both sized resistances dissipate $P^*=0.3P_L$=30 mW. Vectors of identified parameters and corresponding controlled sources are $\mathbf{X}=[R_1R_2]$, $\mathbf{Y_X}=[E_1G_2]$, vector of specified performances $\mathbf{F}^*=[P^*U_2^*]$. Following the proposed methodology, as depicted in Fig.1:

$$\begin{aligned} E_1&=k(P-P^*) &&\rightarrow E_1/k=(P-P^*) \\ G_2&=k(U_2-U_2^*) &&\rightarrow G_2/k=(U-U_2^*) \end{aligned} \qquad (7)$$

and for $k=\infty$: $P=P^*$, $U_2=U_2^*$.

Fig. 5. Voltage divider: adjoint circuit



In PSpice, power dissipated by a single branch: $P=IU$, is modelled by VCVS EMULT. Its output is the product of two input voltages: U and $U'=I$, where U' is the output of CCVS H, controlled by the current I with a unity gain, as shown in Fig. 5. In this exemplary circuit, sum of two EMULT output voltages E_{P1} and E_{P2} is compared with the voltage of $U_P=P^*$ that represents the specified power. The sized resistors are modelled by VCVS E_1 and VCCS G_2 – this second source has to be a current source, to break a voltage source loop. In all exemplary circuits k=10 Meg is assumed. After a single PSpice simulation the following values of resistances have been designated: R_1=185 Ω, R_2=12 kΩ.

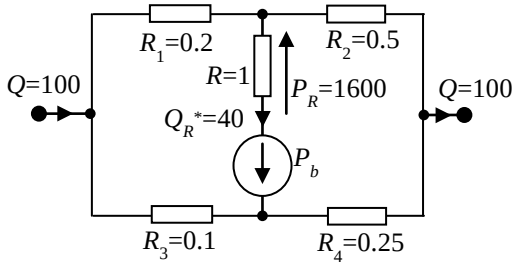
B. Main Ventilation Network

This simple example shows methodology of parameter identification in homogeneous nonlinear ventilation network, sizing of the buster fan pressure and resistance of the regulator for specified airflows is the task. Fig. 6a shows a simplified ventilation network served by a downcast and an upcast shaft,

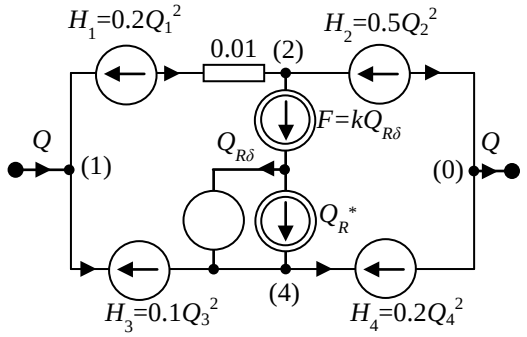
each passing Q=100 m^3/s [6]. The resistance of each subsurface branch is shown. A fan boosts the airflow in the central branch to Q_R^*=40 m^3/s. The task is to determine the total pressure P_b developed by the booster fan. Each resistive branch is described by the following equation (8):

$$P=RQ^2 \ , \text{ where resistance } R \text{ in Pa}\cdot\text{s}^2/\text{m}^6 \qquad (8)$$

The branch of resistance R_i ; i=1,2,3,4, is modelled in PSpice by the polynomial CCVS H_i , as shown in Fig. 6b. The central branch, branch with the sized parameter P_b, is modelled by the CCCS F, controlled by the flow Q_R^*=40 m^3/s. Resistor of 0.01 Ω is connected in series with H_1, to break a loop of voltage sources.



(a)



(b)

Fig. 6. Simplified ventilation network: a) original, b) adjoint

The simulation results, pressures at nodes (1), (2), (4) in Pa, are as follows:

$$\text{(1) } 1363.30 \quad \text{(2) } 415.67 \quad \text{(4) } 1266.2\ 0 \qquad (9)$$

Then,

$$P_b=P_4-P_2+RQ^2=1266.2-415.67+1600=2450 \text{ Pa} \qquad (10a)$$

$$Q_1=68.8 \text{ m}^3/\text{s};\ Q_2=28.8 \text{ m}^3/\text{s};\ Q_3=31.2 \text{ m}^3/\text{s},\ Q_4=71.2 \text{ m}^3/\text{s}$$

This simple problem can be solved algebraically, as shown in [6]. To make this problem more complex, assume that R_1 is the regulated resistance and then, sizing of this resistance together with the booster fan pressure P_b, for the same Q_R^*=40 m^3/s and Q_1^*=68.8 m^3/s, is the task. Now, in the adjoint circuit, branch with the sized resistance and the central branch are modelled by CCCSs, as shown in Fig. 7. The simulation results are the same as given by (9) – the specified flow Q_1^* is the same as the calculated before (10a), for the network of Fig. 6a. The fan pressure P_b is the same, described by equation (10a). The sized resistance is:

$$R_1=(P_1-P_2)/Q_1^*=0.2 \text{ Pas}^2/\text{m}^6 \qquad (10b)$$

i.e. equal R_1 of the Fig. 6a network. That way correctness of the solution has been confirmed. For this problem, the explicit formula (6) is not available. Use of the proposed method allows to find the solution in a single PSpice simulation.

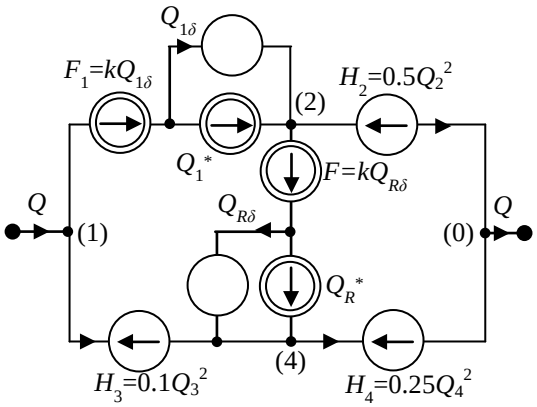
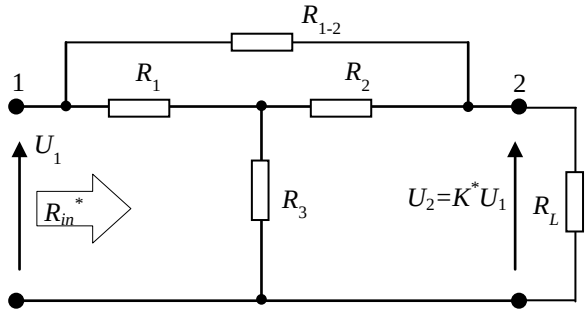


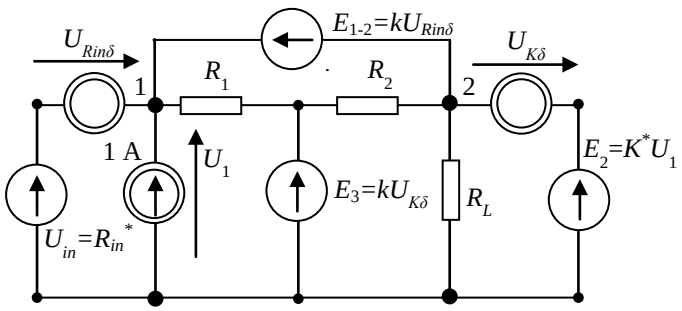
Fig. 7. Ventilation network with a regulator: adjoint circuit

C. Bridged-T Attenuator

This example shows methodology of parameter identification of a passive two-port, for the specified input resistance and the gain. For the Bridged-T Attenuator Circuit shown in Fig. 8a, the task is to size the series bridge resistor R_s=$R_{1\text{-}2}$ and the parallel shunt resistor R_p=R_3, such that the input resistance R_{in}^* is the typical, i.e. the same as R_1=R_2=R_L=8 Ω and the attenuation is K^*=0.1 V/V. In the adjoint circuit, both sized resistors are replaced by VCVCs, controlled by differential voltages designated by R_{in}^* and K^*, as shown in Fig. 8b. The calculated, by PSpice, values of both resistances are: Rs=72 Ω, R_p=0.89 Ω.



(a)



(b)

Fig. 8. Bridget-T Attenuator: a) original, b) adjoint

D. Low-pass Filter

This example shows how to use the proposed method to AC two-port design. In AC circuit design, each specified performance (phasor of voltage or current) and each sized parameter (impedance) are complex numbers. Thus, the sized impedance designates both resistance R (real part) and reactance X (imaginary part), i.e. capacitance or inductance:

$$\text{if } X>0, \text{ then inductance } L=X/(2\pi f) \qquad (11)$$

if $X<0$, then capacitance $C=-1/(X2\pi f)$

In the exemplary low-pass filter loaded by R_L , as shown in Fig. 9a, the task is to size both series and parallel impedance, such that for f^*=1 kHz the following performances are satisfied:

a) the gain is K^*=0.7 V/V and the phase shift between the output voltage and the input voltage is –60° (output voltage lags by 60°), i.e. the output voltage has $U_{out}{}^*=K^*U_{in}$=7 V rms magnitude and –60° phase angle,
b) there is no phase shift between the input voltage and current (pf=1) and the real power dissipated is P^*=1 W, i.e. the input current has $I_{in}{}^*=P^*/U_{in}$=0.1 A rms magnitude and zero phase angle.

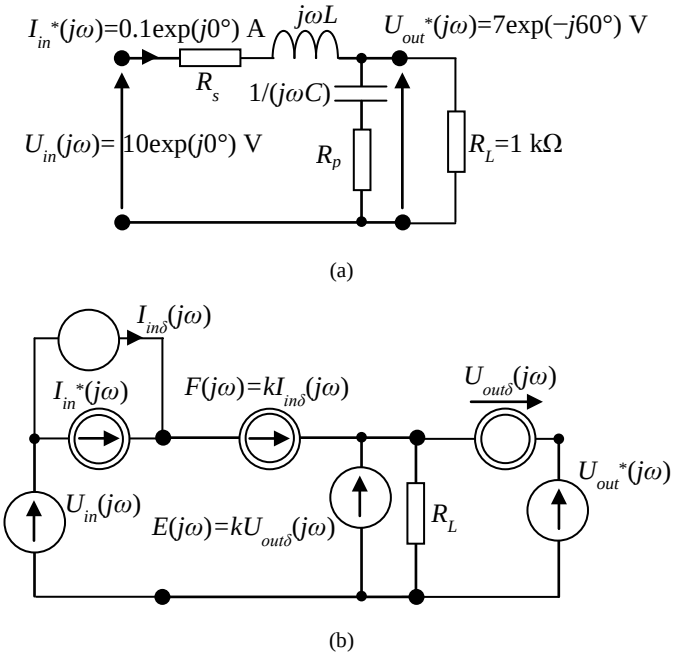


Fig. 9. Low-pass Filter circuit: a) original, b) adjoint

The adjoint circuit is shown in Fig. 9b. The simulation has been run for f^*=1 kHz. The designated values of identified parameters are: L=9.65 mH, R_s=65 Ω, C=2.45 µF, R_p=32.2 Ω.

E. Motor PFC Circuit

This example shows how to use the proposed method to AC two-terminal circuit design. Nameplate-defined data for an induction motor are as follows: rated line voltage U=200 V, frequency f=50 Hz, lagging power factor pf=0.7=cosφ (φ=45.6°), current I_L=14.3 A (real power $P=UI_L$cosφ=2 kW). Identification of the motor inductance L and resistance R, as well as sizing of the PFC capacitance C, is the task. The motor circuit and the corresponding phasor diagram are presented in Fig. 10a. For the properly sized PFC capacitance, the pf is corrected to unity, there is no phase shift between the line voltage $U(j\omega)$ and current $I(j\omega)$. Then, for the rated values of pf and I_L, that designate $I_L{}^*(j\omega)$=14.3exp(−j45.6°) A, the line rms current is $I^*=I_L$cosφ=10 A, as can be examined from the phasor diagram of Fig. 10a. The identified impedances are replaced by CCCSs $F_M(j\omega)$ and $F_{PFC}(j\omega)$, controlled by differential currents:

$I_\delta(j\omega)=I(j\omega)-I^*(j\omega)$, $I_{L\delta}(j\omega)=I_L(j\omega)-I_L{}^*(j\omega)$

with k=10 Meg A/A gain. Please note that use of CCVSs leads to PSpice Error - voltage source loop. The adjoint circuit is presented in Fig. 10b.

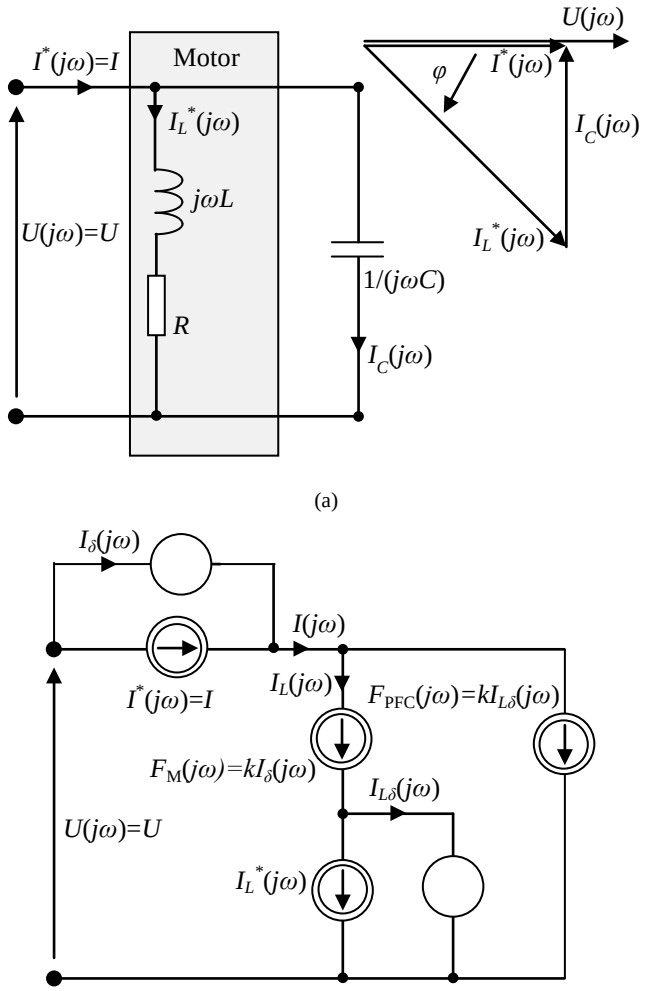


Fig. 10. Low-pass Filter circuit: a) original, b) adjoint

The values of the identified parameters, for the rated frequency f=50 Hz, are: L≈32 mH, R≈10 Ω, C≈162 µF, resistance of the PFC branch is practically zero.

V. Conclusion

The method for sizing analog circuit parameters for the specified design performances, originally proposed in [2] in 1982, has been extended such that performances other than voltage or current: power and transfer function (gain, input impedance, transimpedance), can be considered in both DC and also AC circuit, which is a novel feature. The proposed method utilizes the concept of adjoint circuit in which the

identified element(s) is(are) replaced by controlled source(s) with very high gain (10 Meg). A controlling voltage or current is a difference between the specified and the calculated one. It has been demonstrated, on benchmark example, that such adjoint circuit is practically identical with a circuit obtained from the FNPs method [4]. These two methods differ only in character of an element that produces the controlling variable, but this character is meaningless for the intended PSpice simulation. It should be emphasized, that in the proposed adjoint circuit approach, character of the selected controlled source is absolutely arbitrary, what allows to break a loop of voltage sources or a cutset of current sources, as described in Section IV. In the FNPs method, some moderate difficulties when selecting controlled source other than VCCS may be encountered [4].

The proposed approach is not compared with optimization approaches, approaches that utilize AI tools in optimization process [7,8,9], as simply these approaches can't be competitive with non-heuristic approach! Heuristic approaches can be successfully applied to solve NP-complete problems [10]. The problem of sizing parameters that characterize two-terminal elements, autonomous or being a part of multi-terminal element model, for the given design specifications and $M \leq N$, by means of the adjoint circuit method (same as FNPs method), does not belong to this class. In this method, the solution is found in a single run of PSpice, while heuristic approaches are very time consuming, require multiple simulations and may diverge.

The method can be applied to find mapping described by equation (6), mapping of one point in the performance space into a point in the parameter space or to find approximation of mapping of the feasible region in the performance space into the acceptability region in the parameter space, as initially proposed in [2]. The former case can be utilized in analog fault diagnosis, to identify circuit parameters for the given measurements of selected node voltages. Then, Fault Driven (FD) Simulation After Test (SAT) approach with parameter identification and fault verification can performed [10,11,12]. Many other applications of circuit parameter identification for the specified performances may be enlisted in analog circuit design, such as e.g. postproduction parameter identification, tuning [13] and yield improvement.

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