Derivation of Closed-Form Design Equations for Idealized Operation of Inverse Class-E Power Amplifiers at Any Duty Ratio

Yelin Wang, Suan-Kien Foo and Qibing He

Abstract—Complementary to the conventional class-E topology, inverse class-E operation has several advantages over the class-E counterpart, such as lower peak switch voltage and smaller circuit inductance, which are attractive to high power RF design and MMIC implementation. This paper derives the closed-form design equations that can be used to synthesize the idealized operation of inverse class-E power amplifiers at any switch duty ratio. Calculation of the key design parameters, such as the maximum switch voltage and circuit components values, is elaborated and compared with the case of conventional class-E operation. Further, the theoretical analysis is confirmed and verified by numerical simulations performed on a 500 mW, 2.4 GHz idealized inverse class-E power amplifier.

Keywords—Class-E, power amplifier, numerical simulation.

I. INTRODUCTION

Class-E power amplifier (PA) was first introduced by Sokal in [1]. The design procedure was analyzed and the design equations were derived by Raab in [2]. Class-E amplifier topology is shown in Fig. 1(a). The active device is modeled as a switch and shunted by a capacitor; the operation of the amplifier is tuned by a series LC circuit. The most attractive characteristic of class-E operation is that the efficiency can reach 100 % theoretically. This is attributed to the fact that non-zero values of the voltage across the switch and non-zero values of current flowing through the switch never happen simultaneously. Because of its high efficiency, class-E topology has found its popularity of use in a wide range of applications where the efficiency is one of the most critical requirements, such as PAs, VCOs, supply modulators, AC-AC converters, wireless power transfer (WPT) and so on [3]–[10].

Inverse class-E topology, complementary to class-E, provides another way to realize the similar high efficiency operation and meanwhile shows several attractive advantages. The inverse class-E amplifier topology is illustrated in Fig. 1(b). Differing from the class-E topology, the switch is connected to a series inductor and the circuit is tuned by a parallel LC tank instead. The first advantage lies in the fact that the series inductor can be absorbed into the parasitic inductance of the active device that used as the switch [11]. Second, the peak voltage across the switch is lower than that in the class-E topology, which reduces the risk of breakdown of the active device [11]. Thirdly, the circuit inductance is normally smaller

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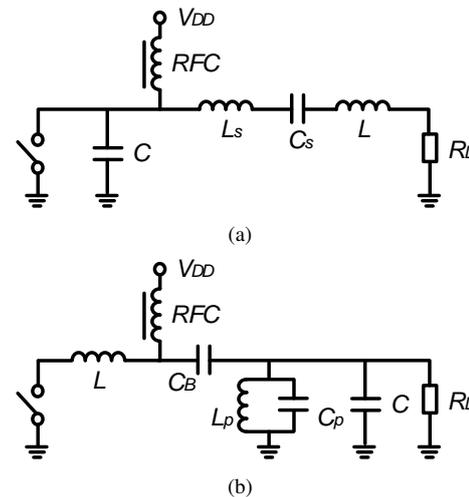
Fig. 1.   Circuit topology of (a) class-E, and (b) inverse class-E power amplifiers.

than that required in class-E topology, which is beneficial to the design of monolithic microwave integrated circuit (MMIC) [12]. For PAs design, most of the literatures in this area study the characteristics of inverse class-E operation only with 50 % nominal switch duty ratio. However, the optimal operation of a practical inverse class-E PA (e.g., in terms of power and efficiency) may depend closely on the duty ratio [13]. This paper presents the derivation of closed-form design equations which can be used to preliminarily synthesize the inverse class-E PAs in their idealized operation mode at any switch duty ratio. Key design parameters, such as the peak voltage across the switch and passive element values, are compared with those in class-E topology. Finally, a 2.4 GHz, 500 mW inverse class-E RF PA is also synthesized and simulated to verify the theoretical analysis.

The paper is organized as follows. In Section II, the derivation of closed-form design equations for synthesis of ideal inverse class-E operation is presented. Switch current and voltage are analyzed in the first place. Then the calculation of passive component values are elaborated. Section III compares important features, such as peak switch voltage and circuit inductance, between inverse class-E and class-E operations. To verify the theoretical analysis in Section II, numerical simulations on a synthesized ideal inverse class-E PA is shown in Section IV. Last, the work is concluded in Section V.
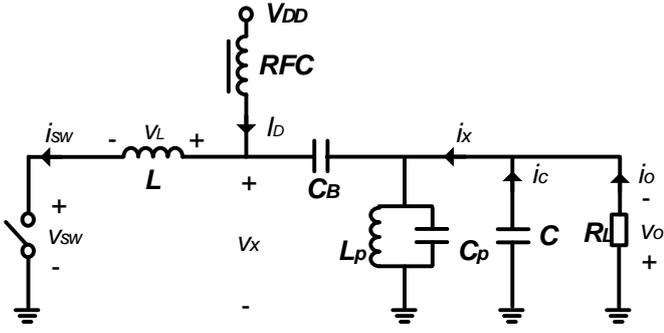
Fig. 2. Inverse class-E amplifier circuit with voltage and current elements noted.

II. DERIVATION OF CLOSED-FORM DESIGN EQUATIONS

A more detailed drawing of an inverse class-E amplifier circuit is shown in Fig. 2, where the important voltage and current elements are noted. The purpose of introducing capacitance C is to compensate for the undesired phase shift at the fundamental frequency. Switching behavior of the active device transforms the supplying DC current, I_D, into a combination of fundamental and harmonic components. The parallel LC circuit (high enough Q-factor is assumed) then filters out the harmonics, generating the fundamental-only current flowing to the load.

To conduct the circuit analysis and keep the simplicity, following operation conditions are assumed:

1) The active device is modeled an ideal switch.
2) An RF-chock (RFC) is used on the supply path to feed DC current to the circuit.
3) All the passive components in the circuit are lossless, i.e., they do not show series equivalent resistance (ESR).
4) The Q-factor (Q_P) of the parallel LC circuit is high enough to guarantee that the amplifier produces sinusoidal signal to the load.

Although various non-ideal factors must be considered in reality, such as the turned-on resistance and output capacitance of the active device, circuit analysis under the ideal condition still plays an important role in the early stage of the amplifier design, i.e., choosing the type and dimension active device and initial values for other circuit components.

A. Analysis of switch current and voltage

Given the parallel LC circuit has high enough quality factor Q_P, the load current and voltage are sinusoidal and can be represented as:

$$i_o(t) = I_o \cdot sin(\omega_c t + \varphi) \tag{1}$$

$$v_o(t) = V_o \cdot sin(\omega_c t + \varphi) \tag{2}$$

where ω_c is the carrier frequency and φ is the phase of the load current and voltage. V_o is equal to $I_o \cdot R_L$. In these two equations, the values of I_o and φ are to be figured out. The basic equation of the circuit is written as:

$$v_X(t) = V_{DD} - v_o(t) \tag{3}$$

When $0 < \omega_c t \le 2\pi D$ (D represents the switch duty ratio and is within the range of (0, 1)), the switch is ON. The switch voltage is 0 and switch current is calculated as:

$$
\begin{aligned}
i_{sw}(t) &= i_L(t) = \frac{1}{L} \cdot \int_0^t v_X(t)dt \\
&= \frac{1}{L} \cdot \{V_{DD}t + \frac{V_o}{\omega_c}[cos(\omega_c t + \varphi) - cos\varphi]\}
\end{aligned} \tag{4}
$$

When $2\pi D < \omega_c t \le 2\pi$, the switch is OFF. In this period, no current flows through the switch and the voltage across the switch is equal to $v_X(t)$. To summarize, the switch current and voltage in the whole range of one switching period are written as Eq. (5) and (6) at the bottom of the page.

The optimum inverse class-E operation can be achieved when the power dissipation due to the ON-OFF transition of the switch is minimized. To realize it, the condition of zero-current-switching (ZCS) and zero-current-derivative-switching (ZCDS) should be fulfilled, represented as:

$$i_{sw}(t)|_{t=\frac{2\pi D}{\omega_c}} = 0 \tag{7}$$

$$\frac{di_{sw}(t)}{dt}|_{t=\frac{2\pi D}{\omega_c}} = 0 \tag{8}$$

Applying Eq. (5) to Eq. (7) and (8), I_o and φ can be figured out:

$$I_o = \frac{2P_o}{V_{DD}} \cdot sin(2\pi D + \varphi) \tag{9}$$

$$\varphi = tan^{-1}[\frac{1 - 2\pi D \cdot sin(2\pi D) - cos(2\pi D)}{2\pi D \cdot cos(2\pi D) - sin(2\pi D)}] + n\pi \tag{10}$$

P_o is the intended output power for the PA to be designed.

The peak switch current and voltage are important parameters in class-E amplifier design. They provide the guidance to choose the proper type and size of the active device to ensure reliable operation of the circuit. By using Eq. (5), (6), (9), (10), the values of these two parameters can be figured out. The peak switch current is:

$$i_{sw,pk} = \frac{V_{DD}}{\omega_c L} \cdot \{sin^{-1}(\frac{1}{\beta}) + \beta cos[sin^{-1}(\frac{1}{\beta})] - \beta cos\varphi - \varphi\} \tag{11}$$

$$i_{sw}(t) = \begin{cases} \frac{1}{L} \cdot \{V_{DD}t + \frac{V_o}{\omega_c}[cos(\omega_c t + \varphi) - cos\varphi]\} & \text{if } 0 < \omega_c t \le 2\pi D \\ 0 & \text{if } 2\pi D < \omega_c t \le 2\pi \end{cases} \tag{5}$$

$$v_{sw}(t) = \begin{cases} 0 & \text{if } 0 < \omega_c t \le 2\pi D \\ V_{DD} - I_o \cdot R_L \cdot sin(\omega_c t + \varphi) & \text{if } 2\pi D < \omega_c t \le 2\pi \end{cases} \tag{6}$$

which occurs at the time instants:

$$t_{ipk} = \frac{1}{\omega_c} \cdot [sin^{-1}(\frac{1}{\beta}) - \varphi + 2n\pi] \tag{12}$$

And peak switch voltage is:

$$v_{sw,pk} = V_{DD} \cdot (1 + \beta) \tag{13}$$

which occurs at the time instants:

$$t_{vpk} = \frac{1}{\omega_c} \cdot (\frac{3\pi}{2} - \varphi + 2n\pi) \tag{14}$$

β in Eq. (11), (12), (13) is the ratio between V_o and V_{DD}:

$$\beta = \frac{V_o}{V_{DD}} = \frac{1}{sin(2\pi D + \varphi)} \tag{15}$$

B. Calculation of circuit component values

The switch current has been previously calculated as shown in Eq. (5). However, the inductance L in Eq. (5) still needs to be determined. To calculate the values for the circuit components, such as L and C in Fig. 2, the switch current shown in Eq. (5) is first rewritten as a Fourier series:

$$i_{sw}(t) = A + \sum_{n=1}^{N}[a_n \cdot cos(n \cdot \omega_c t + \varphi) + b_n \cdot sin(n \cdot \omega_c t + \varphi)] \tag{16}$$

From Fig. 2, it is obvious that the fundamental component of Eq. (16) is equal to $i_X(t)$ given a high enough Q_P of the parallel LC tuned circuit. From this perspective, following equation can be obtained:

$$I_D + i_X(t) = A + [a_1 \cdot cos(\omega_c t + \varphi) + b_1 \cdot sin(\omega_c t + \varphi)] \tag{17}$$

where I_D is the DC current fed to the circuit, A, a_1 and b_1 are coefficients of the Fourier series and can be calculated using the expression of the switch current shown in Eq. (5) as Eq. (18) to (20) at the bottom of the page.

From another angle, it is evident from Fig. 2 that $i_X(t)$ is the sum of $i_c(t)$ and $i_o(t)$, so that:

$$i_X(t) = \omega_c C \cdot V_o \cdot cos(\omega_c t + \varphi) + I_o \cdot sin(\omega_c t + \varphi) \tag{21}$$

Comparing Eq. (17) and (21) and using Eq. (19) and (20), values of L and C can be obtained:

$$L = \frac{1}{\pi\omega_c} \cdot \frac{V_{DD}^2}{2P_o} \cdot [1 + 2(\pi D)^2 - \beta(sin\varphi + 2\pi D cos\varphi)] \tag{22}$$

$$C = \frac{1}{2\pi} \cdot \frac{1}{\omega_c^2} \cdot \frac{1}{L} \cdot [(1 - \frac{1}{\beta^2}) \cdot 2\pi D - \frac{1}{\beta}cos\varphi + sin\varphi cos\varphi] \tag{23}$$

Last, values of L_P and C_P in the parallel LC tuned circuit can also be figured out given a quality factor of Q_P:

$$L_P = \frac{R_L}{\omega_c Q_P} = \frac{1}{\omega_c Q_P} \cdot \frac{\beta^2 V_{DD}^2}{2P_o} \tag{24}$$

$$C_P = \frac{Q_P}{\omega_c R_L} = \frac{Q_P}{\omega_c} \cdot \frac{2P_o}{\beta^2 V_{DD}^2} \tag{25}$$

III. COMPARISON BETWEEN CLASS-E AND INVERSE CLASS-E OPERATION

Ideal inverse class-E and class-E power amplifiers (i.e., fulfilling the four assumptions described early) both have 100 % efficiency theoretically. Due to the difference in their circuit topologies, they have some different features which are essential to be noticed. Based on the closed-form design equations for class-E PA derived in [13], and for inverse class-E PA derived in this work, some key design parameters of these two topologies are compared in this section.

Fig. 3 plots the theoretical peak current flowing through the switch for both class-E and inverse class-E PAs. Peak switch current normalized to the DC current fed into the circuit, $i_{sw,pk}/I_D$, versus the switch duty ratio, D, is plotted. From the figure, it can be seen that for both class-E and inverse class-E operation, the duty ratio should be larger than 0.3 in order to keep the peak switch current under a reasonable level, e.g., 6 times DC current. It can also be observed that the peak switch current in inverse class-E operation is always larger than that in class-E operation, when the duty ratio is larger than 0.3.

Similarly, Fig. 4 compares the normalized peak voltage, $v_{sw,pk}/V_{DD}$, across the switch between class-E and inverse class-E operation. Peak switch voltage is one of the most critical element to be considered in the design of class-E and

$$
\begin{aligned}
I_D = A & = \frac{\omega_c}{2\pi} \cdot \int_0^{\frac{2\pi}{\omega_c}} i_{sw}(t)dt \\
& = \frac{1}{2\pi} \cdot \frac{V_{DD}}{\omega_c L} \cdot [1 + 2(\pi D)^2 - \beta \cdot (sin\varphi + 2\pi D cos\varphi)]
\end{aligned}
\tag{18}
$$

$$
\begin{aligned}
a_1 & = \frac{\omega_c}{\pi} \cdot \int_0^{\frac{2\pi}{\omega_c}} [i_{sw}(t) \cdot cos(\omega_c t + \varphi)]dt \\
& = \frac{1}{\pi} \cdot \frac{V_{DD}}{\omega_c L} \cdot \{(\frac{2}{\beta} + \beta) \cdot \pi D - 2cos\varphi + \frac{\beta}{4}sin(2\varphi) + \frac{3}{2}cos[sin^{-1}(\frac{1}{\beta})]\}
\end{aligned}
\tag{19}
$$

$$
\begin{aligned}
b_1 & = \frac{\omega_c}{\pi} \cdot \int_0^{\frac{2\pi}{\omega_c}} [i_{sw}(t) \cdot sin(\omega_c t + \varphi)]dt \\
& = \frac{1}{\pi} \cdot \frac{V_{DD}}{\omega_c L} \cdot \{\frac{3}{2\beta} - \frac{\beta}{2} - sin\varphi - \frac{\beta}{2}cos^2\varphi - (2\pi D - \beta cos\varphi) \cdot cos[sin^{-1}(\frac{1}{\beta})]\}
\end{aligned}
\tag{20}
$$
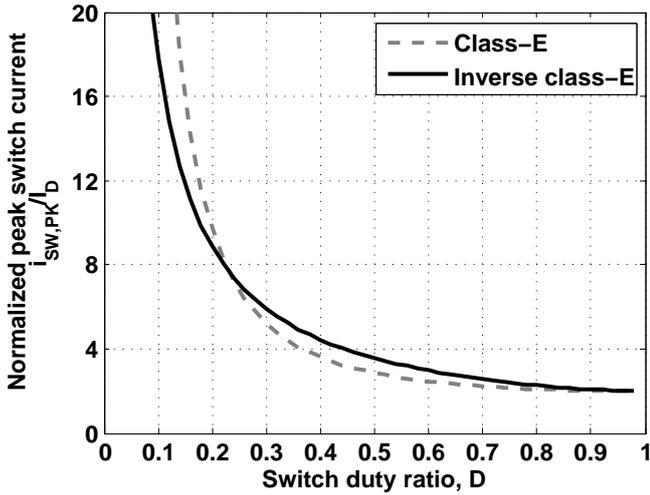
Fig. 3.   Comparison of normalized peak switch current between class-E and inverse class-E operation.
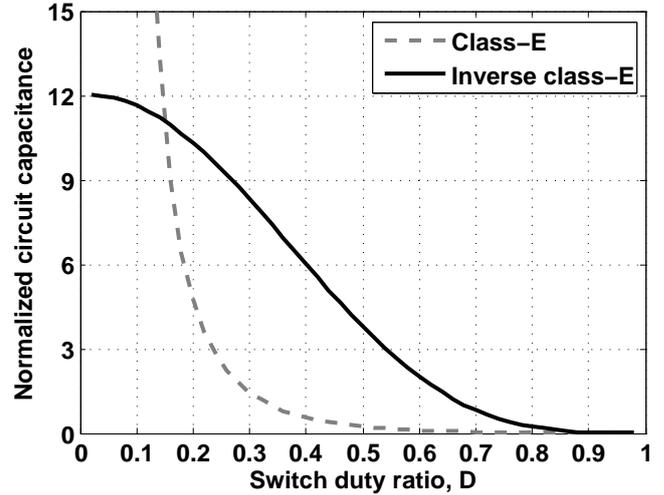
Fig. 5.   Comparison of normalized circuit capacitance between class-E and inverse class-E operation.
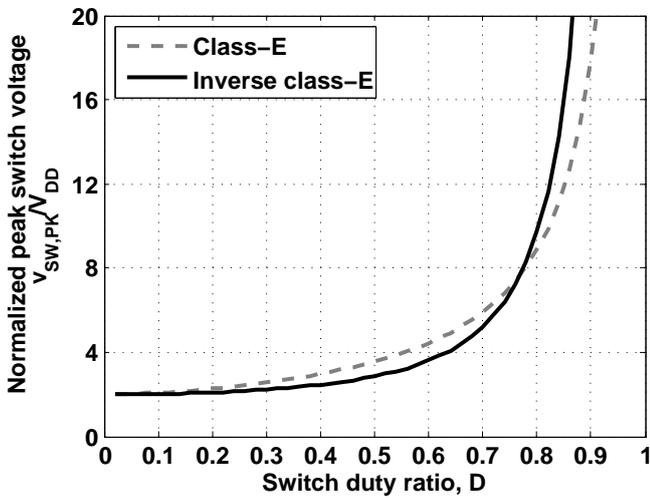
Fig. 4.   Comparison of normalized peak switch voltage between class-E and inverse class-E operation.
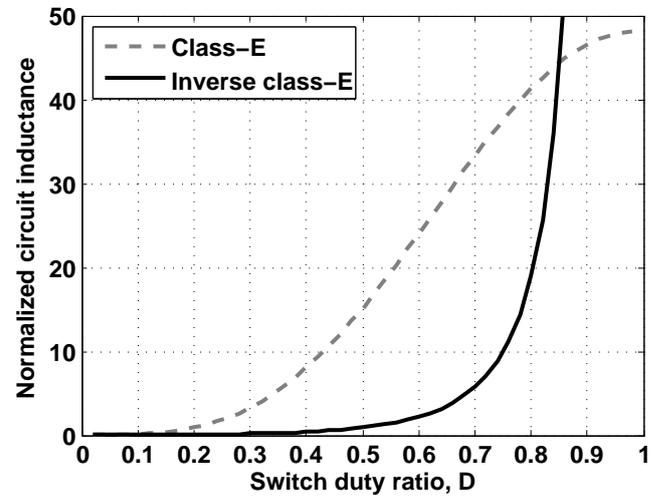
Fig. 6.   Comparison of normalized circuit inductance between class-E and inverse class-E operation.

inverse class-E PAs. From the figure, it can be seen that the peak switch voltage is always larger than 2 times the supply voltage. To ensure reliable and safe circuit operation, namely, to prevent the active device (the switch) from breakdown, the supply voltage should be chosen at a level which is considerably lower than the device breakdown voltage [14], [15]. In addition, compared to other technologies, this issue is especially critical in CMOS because of its relatively low breakdown voltage [16]–[19]. From the figure, it is seen that the peak switch voltage will become unreasonably high when the duty ratio increases toward 1 for both circuit operation. It can also be observed that the peak switch voltage of inverse class-E operation is always lower than that of class-E operation, when the switch duty ratio is smaller than, e.g., 0.75. This is one of the attractive advantages of the inverse class-E operation over the class-E counterpart.

Fig. 5 and Fig. 6 compare the circuit capacitance and inductance between class-E and inverse class-E operation, respectively. Referring to Fig. 1, the circuit capacitance of class-

E and inverse class-E topologies are $C + C_s$ in Fig. 1(a), and $C + C_p$ in Fig. 1(b), respectively. In Fig. 5, these capacitance are normalized to $((2P_o)/V_{DD}^2)/\omega_c$ (referring to Eq. (23)). Remember that P_o is the intended output power. Similarly, the circuit inductance of the two topologies are $L + L_s$ in Fig. 1(a), and $L + L_p$ in Fig. 1(b), respectively. In Fig. 6, these inductance are normalized to $(V_{DD}^2/(2P_o))/\omega_c$ (referring to Eq. (22)). Same quality factor of the series (in class-E) and parallel (in inverse class-E) tuned LC circuit is assumed. From Fig. 5, it is observed that the circuit capacitance of class-E operation keeps at a relatively low value when compared to the case of inverse class-E operation, especially if the switch duty ratio is higher than, e.g., 0.3.

In contrast, the comparison of circuit inductance between the two topologies shows an opposite situation, as plotted in Fig. 6. When the switch duty ratio is smaller than, e.g., 0.8, the circuit inductance of inverse class-E operation is much smaller than that of class-E counterpart. On-silicon inductor design normally presents a problem in the design of fully integrated

TABLE I
COMPARISON OF THEORETICAL CIRCUIT PARAMETERS BETWEEN CLASS-E AND INVERSE CLASS-E OPERATION

	$D=0.4$		$D=0.5$		$D=0.6$	
	Class-E	Inverse class-E	Class-E	Inverse class-E	Class-E	Inverse class-E
I_D [mA]	227.8	227.8	227.8	227.8	227.8	227.8
$v_{sw,pk}$ [V]	5.36	4.43	6.41	5.15	8.00	6.50
$i_{sw,pk}$ [A]	1.00	1.24	0.80	0.99	0.68	0.83
V_o [V]	1.38	2.63	1.93	3.35	2.47	4.70
I_o [A]	0.72	0.38	0.52	0.30	0.41	0.21
R_L [Ω]	1.91	6.91	3.74	11.23	6.08	22.04
L [nH]	0.21	0.05	0.29	0.14	0.33	0.36
L_s or L_p [nH]	1.52	0.04	2.97	0.06	4.84	0.12
C [pF]	8.47	7.76	3.26	6.80	1.14	5.06
C_s or C_p [pF]	2.90	115.2	1.48	70.83	0.91	36.1

circuits and systems, e.g., MMIC [20], [21]. One reason is that on-chip passive inductors occupy a significant die area making the whole design impractical. The other reason is their relatively low quality factor due to the parasitic losses on the substrate [20], [22]. It can be seen from Fig. 6 that the circuit inductance in inverse class-E operation keeps itself at rather a low level comparing to the class-E topology, especially when the switch duty ratio is under 0.7. This attractive advantage of inverse class-E topology makes it promising to implement fully on-silicon circuits and systems, such as transceivers, of which many building blocks are efficiency-critical and inductance is essential, e.g., PAs, VCOs, supply modulators, etc [3]–[8].

To have a more quantitative overview on the comparison between the class-E and inverse class-E operation, Table I lists the value of peak current and voltage, and passive components in the circuits of both topologies under the condition: $D=0.4$, 0.5 and 0.6, $V_{DD}=1.8$ V, $P_o=500$ mW, $\omega_c=2\pi\cdot2.4$ GHz and Q_S or $Q_P=12$.

IV. NUMERICAL SIMULATION RESULTS

Previous sections present the derivation of the closed-form design equations for the synthesis of idealized inverse class-E operation, as well as the graphic illustration of those derived equations. To preliminarily verify the theoretical analysis, in this section, an ideal inverse class-E amplifier is synthesized and simulated in Agilent Advanced Design Systems (ADS).

The amplifier operates with a carrier frequency of 2.4 GHz and a DC supply of 1.8 V. The intended output power of the amplifier is 500 mW and the quality factor Q_P of the parallel LC circuit is assumed to be 12. The active device is modeled as a ideal voltage controlled switch (a component in ADS), where the OFF resistance is infinity and the ON resistance is set at 0.01 Ω. Different switch duty ratio D is tested. The switch current and voltage, output current and voltage are plotted to verify the theory. The values of circuit components are set as calculated from the designed equations derived previously. From these figures, an excellent agreement can be observed between the theoretical analysis and the accordingly simulation. The shape of the switch current and voltage
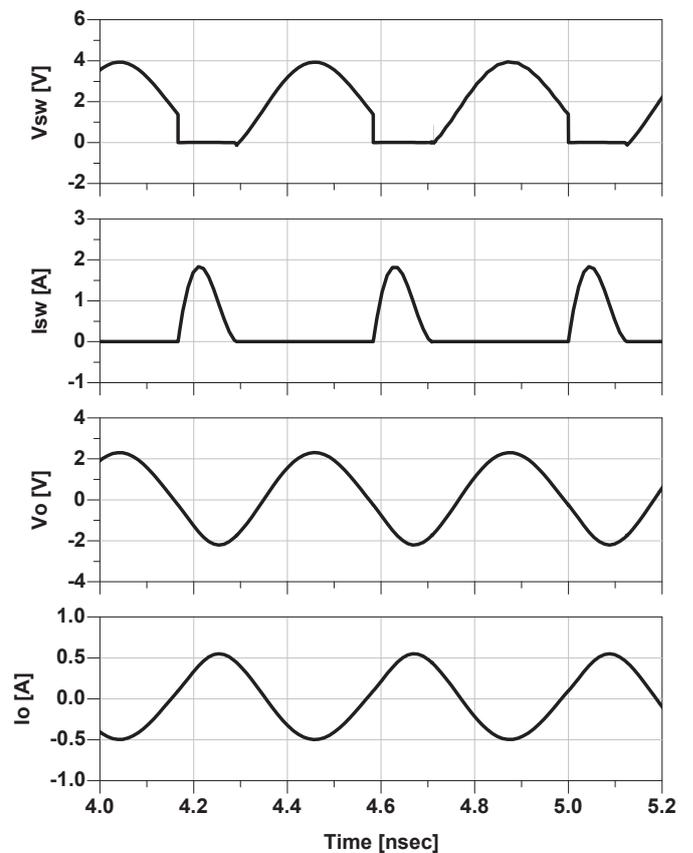
Fig. 7. Simulated current and voltage waveforms with switch duty ratio $D=0.3$.

are realized as desired and the 100%-efficiency operation is achieved as expected (i.e., non-zero switch current and voltage never occur simultaneously).

V. CONCLUSION

This paper presents the derivation of closed-form design equations for ideal inverse class-E operation at any switch duty ratio. An idealized 2.4 GHz, 500 mW inverse class-E power amplifier is then synthesized and simulated in ADS. The theory is successfully verified by comparing the simulated time-domain circuit current/voltage waveforms to the theoretical
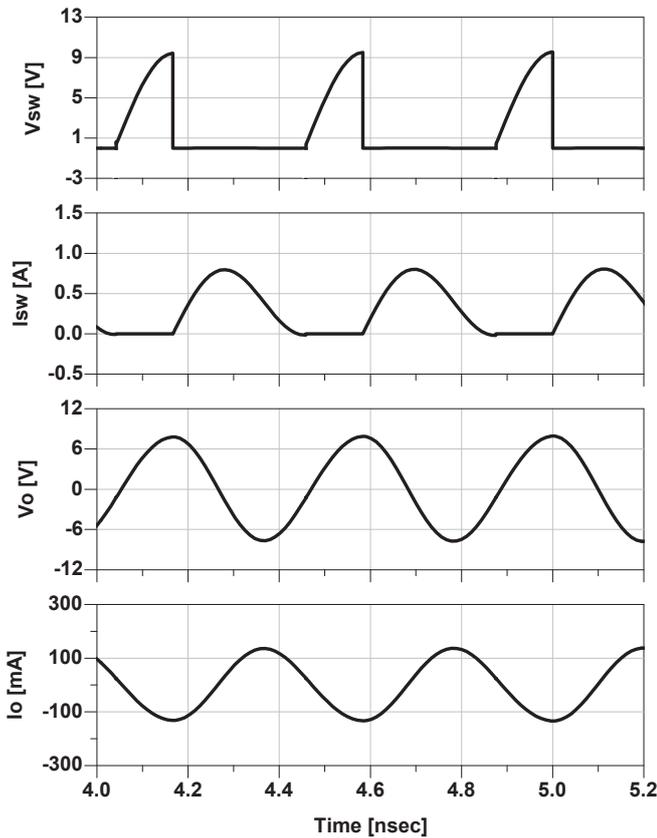
Fig. 9.   Simulated current and voltage waveforms with switch duty ratio D=0.7.
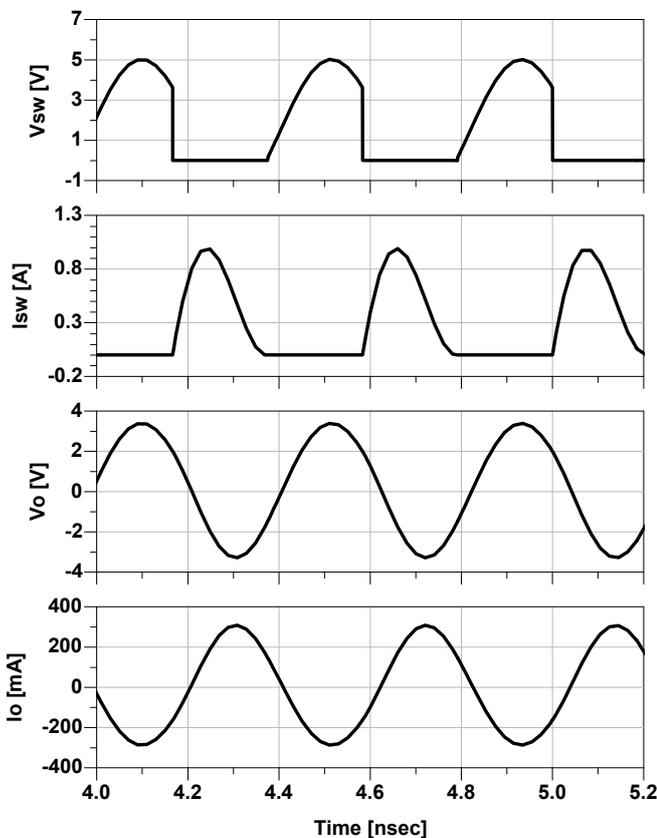
Fig. 8.   Simulated current and voltage waveforms with switch duty ratio D=0.5.

calculation. What's more, the feature of inverse class-E operation is compared with that of class-E counterpart in terms of the key design parameters, such as peak switch current/voltage and values of circuit capacitance and inductance. Based on the comparison, the significant advantages of inverse class-E over class-E operation are studied and illustrated. All the study in this work are conducted based on the assumption of ideal inverse class-E operation. However, the work still provides a quick and important guidance to the initial design of inverse class-E power amplifiers, e.g., choosing the initial dimension of the active device, setting the initial values for the passive components in the circuit, etc. Based on the fundamental study presented in this work, further research will focus on analyzing the design of inverse class-E amplifier in a more practical sense. The effects of finite DC-feed inductor, non-ideal switching behavior and parasitics of active device, and undesired power dissipation on the lossy passive components will be investigated more deeply.

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