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Low-Power High-Speed Double Gate 1-bit Full Adder Cell

Raushan Kumar, Sahadev Roy, and C.T. Bhunia

***Abstract*— In this paper, we proposed an efficient full adder circuit using 16 transistors. The proposed high-speed adder circuit is able to operate at very low voltage and maintain the proper output voltage swing and also balance the power consumption and speed. Proposed design is based on CMOS mixed threshold voltage logic (MTVL) and implemented in 180nm CMOS technology. In the proposed technique the most time-consuming and power consuming XOR gates and multiplexer are designed using MTVL scheme. The maximum average power consumed by the proposed circuit is 6.94µW at 1.8V supply voltage and frequency of 500 MHz, which is less than other conventional methods. Power, delay, and area are optimized by using pass transistor logic and verified using the SPICE simulation tool at desired broad frequency range. It is also observed that the proposed design may be successfully utilized in many cases, especially whenever the lowest power consumption and delay are aimed.**

***Keywords*— Low-power full-adder, Low-power CMOS design, multiplexer based full-adder design, multi-threshold voltage based Full-adder design, pass transmission logic.**

I. INTRODUCTION

A Large numbers of transistors are required to integrate onto a single chip to perform various complex operations. As the level of integration increases, different design challenges need to be considered. Major design challenge is related to the decreasing dimensions of on-chip components and for the associated interconnection's length decrement. As the number of transistors is increase in any electronics system raised power consumption, propagation delay, area and the design process became difficult and more efficient design methods is required. CMOS mainly consumed maximum power in any VLSI circuits. There are many power consumption factors like switching power dissipations due to switching activity of node capacitance, short circuits power due to the current flow from the power supply to ground and static power consumptions due to the leakage current of CMOS. The general method for power consumption minimizations is scaling of supply voltage and capacitance load of the VLSI circuit. Power dissipation of any circuits is influenced by the logic style chosen by the designer [1]. One of the basic building blocks of any VLSI circuit is the single-bit adder. The addition of one-bit binary number is fundamental and quickly used in any arithmetic operations. Design standards of a full adder circuit are reducing transistor count, power consumption, and delay factors [2]. Another important part often conflicting with design standards are power consumption and speed, i.e. power-delay-product (PDP) [3]. Those designs are focusing on many logic styles like static CMOS, dynamic-transmission gate, pass transistor logic, reversible logic, etc. The typical complementary CMOS (C-CMOS) full-adder design using 28 transistors with an equal number of PMOS and NMOS is reported in [4]. PMOS transistors are used to design pull up circuits, and NMOS are used to design pull down operations. In this type of design methodology, due to the cascading output stage, additional buffers are essential to provide required driving power. Hence, the number of transistors increased. Another alternative design approach is complementary pass-transistor logic (CPL) using 32 transistors having the better driving ability, but required high-power [5]. The different pass transistor logic (PTL) [6, 7] families are used in many integrated circuits by eliminating redundant transistors and this technique effectively reduced transistor count. Other popular design methods are using transmission gate, where minimum 20 transistors are required [8]. Static energy recovery full adder (SERF) with ten transistors is work based on PTL. The Advantages of these circuits is less power consumption, but delay increased due to XOR/XNOR module [9, 10]. Hybrid 1-bit full adder with 16 transistors consists of three blocks. Where two blocks are the XNOR modules used to generate the sum signal (SUM) and other used to produce the carry [11]. In double gate 20-transistor based adder circuit the front and back gates are attached to reduce the sub-threshold leakage and short channel effect, and these two gates lead to the increase the current driving capability of DG CMOS. Hence, the circuit with DG transistor can be operated used threshold voltages compared to planar CMOS circuit. These are useful for low power and high-speed circuits in [12]. A new 16 transistor full adder design reported in [13] using flexible design method the basic design of the whole full adder it is realized by two six transistors XNOR and one 2:1 multiplexer. This high-speed design can provide the output, with proper voltage swing for the low supply voltage. The direct path between supplies voltage to ground may be eliminated by using multiplexer based full adder (MBA). This type of design approach required 12 transistors only but unsuitable for cascade mode operation [14].

The proposed 16T double gate full adder circuit is designed using the mixed threshold voltage logic (MTVL) scheme using 180nm CMOS technology. The proposed circuit consumed low-power due to minimum leakage current and also it is

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suitable for high-speed operations in contrast to other design methodologies.

The whole paper is organized as follows: method and mechanisms of power ingestion are in section (II). The design procedure of the new low power high-speed 16T 1-bit full adder cell is a section (III). Simulation results of proposed full adder circuit are analyzed in the section (IV), and some conclusions and future research directions are summarized in section (V).

II. Method and Mechanisms of Power Ingestion

The threshold voltage (V_T) controlled parameters of any CMOS transistor are: (i) work function difference between gate and channel (ϕ_{gc}), (ii) changing of gate voltage due to the surface potential (ϕ_f), (iii) substrate bias voltage (V_{SB}) and (iv) offset voltage [15]. The generalized form of the threshold voltage can also be written as in Equation (1).

$$V_T = V_{T0} - \frac{Q_d - Q_{d0}}{C_{ox}}$$

$$\text{Or, } V_T = V_{T0} + \gamma\left(\sqrt{|V_{SB} - 2\phi_f|} - \sqrt{|2\phi_f|}\right) \quad (1)$$

Where $V_{T0} = \emptyset_{GS} - 2\emptyset_F - \frac{Q_{d0}}{C_{ox}} - \frac{Q_i}{C_{ox}}$

γ is a body effect coefficient:

$$\gamma = \frac{\sqrt{2q\,N_A\,\in_{si}}}{C_{ox}} \quad (2)$$

where q, the electron charge; N_A, density of doped carriers; $\in_{si}$, permeability of silicon; C_{ox}, gate oxide capacitance per unit area.

The power dissipation of any digital VLSI circuits is mainly classified as dynamic power dissipations and static power dissipations. The causes of dynamic power dissipation are due to switching power dissipation and short-circuit power dissipation when the logic level changes. Static power dissipations occurred due to diode leakage current [16]. In CMOS fixed power is quite small because of consideration of sub-micron technology. Reduction in short circuit power consumption and static power consumption is indication for a reduction in power consumption without degrading drivability of the circuit [17]. The total power consumption (P_{total}) may be considered as switching power consumption (P_{sw}), short circuit power dissipation (P_{skt}) and leakage power consumption (P_{lek}) due to leakage current (I_{lek}) is given by,

$$P_{total} = P_{sw} + P_{skt} + P_{lek} \quad (3)$$

$$P_{total} = V_{dd} f_{clk} \sum \gamma V_{sw} C_l + V_{dd}\, f_{clk} \sum I_{sc} + I_{lek}\, V_{dd} \quad (4)$$

where V_{dd}, power supply voltage; V_{sw}, voltage swing of the output is equal to power supply; C_l , load; f_{clk}, system clock frequency; I_{sc} , short-circuit current at that node.

Another important parameter is propagation delay. The propagation delay time is calculating low to high and high to the low output of the transition. The time delay average represented as,

$$\tau_{average} = \frac{\tau_{PHL} + \tau_{PLH}}{2} \quad (5)$$

$$\tau_{PHL} = \frac{C_{load} \cdot \left(\frac{V_{dd}}{2}\right)}{KW\,(V_{DD} - V_{th})} \quad (6)$$

Where

τ_{PHL} = propagation delay for switching the output voltage from high to low;

τ_{PLH} = propagation delay for switching the output voltage from low to high;

K= a factor which depends on carrier saturation velocity, the channel length, and the degree of velocity saturation;

W = channel width.

When input voltage switches from high to low, and low to high during this phase, the output of load capacitance load is being charged up. Therefore, capacitor current equals to the instantaneous drain current of the transistor, therefore, periodic input-output waveforms generated due to load capacitance and average power dissipated by one period is given below,

$$P_{avg} = f C_{load}\, V_{dd}^2 \quad (7)$$

Here, f is the clock frequency of switching activity of any complete cycle. One of the ways to minimize the dynamic power dissipation is by reducing the supply voltage. When supply voltage (V_{dd}) is below 1V circuit performance starts degrading [18]. The overall performances at low-voltage are possible to improve by reducing V_{th}. However, V_{th} has a direct impact on leakage current, which affected many designed parameters. We can overcome this problem by optimizing all design parameters, and the proposed model worked satisfactorily in the range from 0.8V to 1.8V.

III. Design Procedure of Proposed Full Adder

A. Proposed mixed threshold CMOS XOR gate

The basic full adder circuit is modified using a concept of the mixed threshold voltage scheme to operate successfully at both high and low threshold voltage. For higher Vth, leakage current can be reduced but performance is degraded. However, at low-Vth operation, transistors give better performances but have a leakage current increase. The proposed design perfectly balances both by using different threshold voltage. The variation of the threshold voltage is realized due to a change in channel length and channel width of the CMOS transistor. When the transistors are in a stack, their channels are too close to each other. It also increased the difficulty in distinct channel doping. More explicit instruction is required. Mixed threshold CMOS design schemes may be classified into two categories MVTI and MTV2. In MTV1 scheme, both p pull-up and n pull-down blocks are operated in different threshold voltage. In MVT2 scheme, CMOS worked in distinct threshold voltage and were suitable to use any circuit unless transistors are connected in series. The XOR blocks of the proposed full adder are designed based on MTV2 scheme (Fig.1). Here two CMOS (P1 and N1) are working in high threshold voltage, and another two CMOS (P3 and N3) are working at a low-threshold voltage.

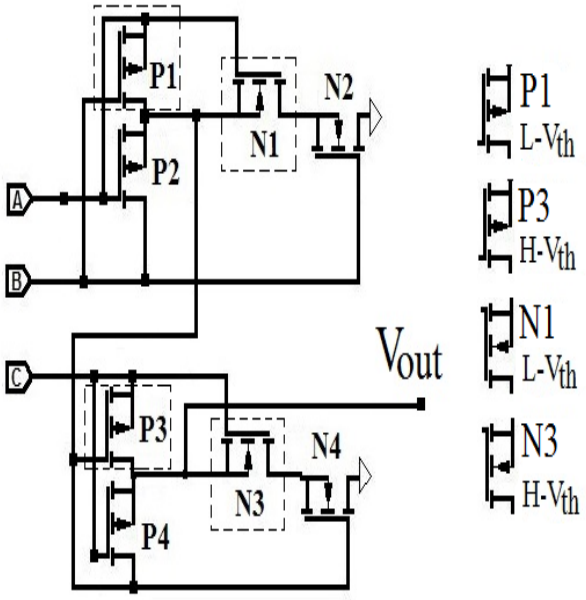

Fig. 1. MTV SCHEME.

B. *Design Style of the Proposed Full Adder*

The proposed adder circuit is designed using a modular approach scheme. It consists of two XNOR module and one multiplexer block (Fig. 2).

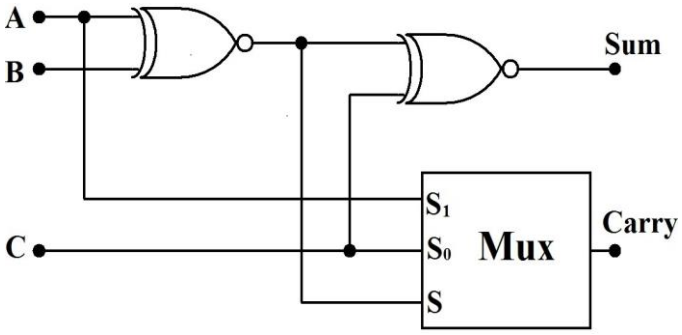

Fig. 2. Block diagram of 16T full adder.

In a given circuits of full adder the sum output is obtain by two series connected MTV logic XNOR gate. XOR blocks are realized using six multi-threshold CMOS transistors and 2:1 mux designed using 4 CMOS transistors as shown in the Fig. 3. Layout view of the proposed circuit is shown in Fig. 4. The proposed multiplexer has two input lines: S0 (Cin) and S1 (A). Carry output is generated depending on the logic value of the select line (A⊕B).When the both inputs (A, B) are same, it becomes high then multiplexer passes A, in other cases Cin. Truth table of the multiplexer shown in the Table I. The proposed design satisfied the basic operation of a full adder given by the equation (8) and (9).

$$Sum = A \oplus B \oplus Cin \quad (8)$$

$$Carry = AB + BCin + ACin \quad (9)$$

Here, A, B and Cin indicate two inputs of the circuit and previous input carry.

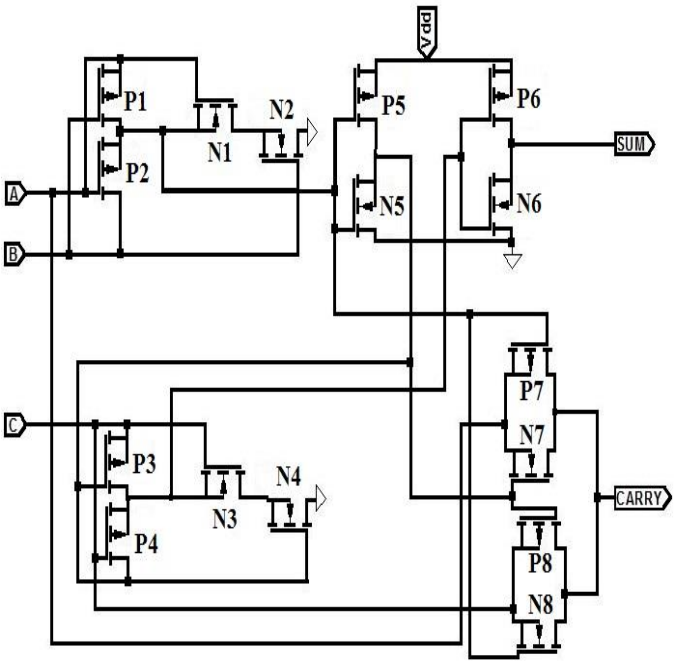

Fig 3. 16T double gate full adder circuit.

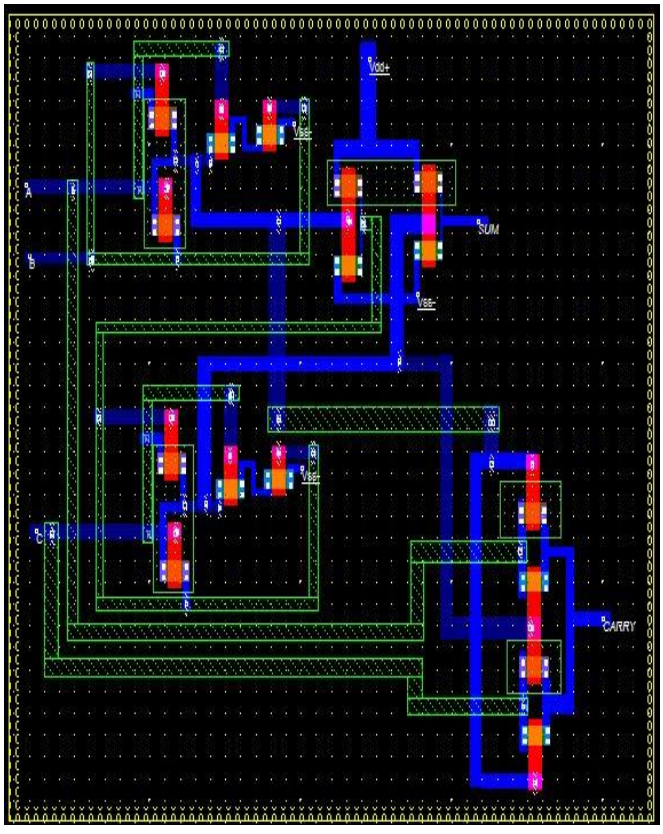

Fig. 4. Layout of 1-bit double gate full adder using180nm technology.

IV. Result Analysis

The overall performance of the proposed full-adder cell (Fig. 3) is evaluated in this section and also compared with the other traditional model. The adder cells are simulated using 180nm CMOS technology within the frequency range 100 to 500MHz.

TABLE I
INPUT OUTPUT TABLE OF MULTIPLEXER

Input Combinations			Sum	Carry	Select Line $S = A \oplus B$	Mux Output
A	B	C				$AS + C\bar{S}$
0	0	0	0	0	1	0
0	0	1	1	0	1	0
0	1	0	1	0	0	0
0	1	1	0	1	0	1
1	0	0	1	0	0	0
1	0	1	0	1	0	1
1	1	0	0	1	1	1
1	1	1	1	1	1	1

The overall per performance of proposed design is simulated in different frequency range between 100MHz to 500MHz at different supply voltage ranging from 0.8V to 1. 8V. A single-bit full adder cell may perform well in simulations, but it failed upon actual deployment. Driving power is degraded due to the cascading arithmetic circuits. It is essential that it can provide proper inputs to the next cell. The performance of the cascade circuit will be degraded or become non-operative at low supply voltage if the driving unit does not provide full swing outputs to the driven cells (Fig. 5). Additional buffers are essential at output stages to improve the performance of TFA, TGA, 14T, and 10T adder cells [11]. Hence, cascade adders using proposed methodology are used here to check its actual performance. It is observed that the proposed full adder is capable of cascade operation without degrading its performance.

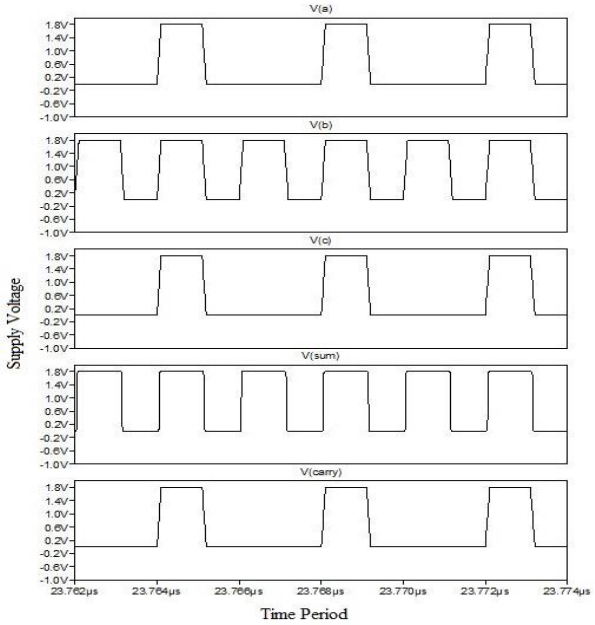

Fig. 5. Input and output pattern of the simulation result.

TABLE II
PERFORMANCE ANALYSIS OF THE PROPOSED FULL ADDER CIRCUITS

Power Supply(V)	Frequency (MHz)	Average power (µw)	Delay (ns)	PDP (f j)
0.8	100	0.291	0.5982	0.174
	200	0.325	0.5724	0.186
	300	0.335	0.5714	0.191
	400	0.345	0.5632	0.194
	500	0.358	0.5602	0.201
1.0	100	1.11	0.1924	0.213
	200	1.11	0.1675	0.185
	300	1.16	0.1424	0.165
	400	1.21	0.1402	0.169
	500	1.53	0.1506	0.230
1.2	100	2.11	0.1868	0.394
	200	2.11	0.1545	0.326
	300	2.18	0.1478	0.322
	400	2.25	0.1396	0.314
	500	2.50	0.1481	0.370
1.4	100	3.29	0.1759	0.578
	200	3.32	0.1534	0.509
	300	3.57	0.1461	0.521
	400	3.65	0.1358	0.495
	500	3.95	0.1402	0.553
1.6	100	3.95	0.1626	0.642
	200	4.02	0.1512	0.607
	300	4.27	0.1437	0.613
	400	4.80	0.1349	0.647
	500	5.11	0.1367	0.698
1.8	100	4.05	0.1590	0.644
	200	4.11	0.1497	0.615
	300	4.83	0.1420	0.685
	400	5.95	0.1293	0.769
	500	6.94	0.1336	0.927

A. Variation with voltage

Power consumption and power-delay-product depend on operating voltage and frequency. It is observed that average power increases with supply voltage as shown Fig. 6. The average power consumption of the proposed full adder is less than 30% in comparison with static CMOS inverter based full adder [11]. Hence, this MTV based full adder is the most suitable for ultra-low power circuits designing.

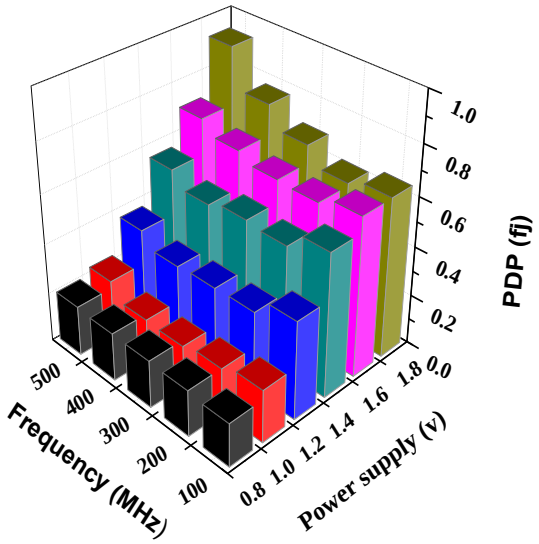

Fig. 6. Power delay product with supply voltage.

B. *Variation with frequency*

The proposed circuit is also analysed at different frequencies (100MHz to 500MHz). As the frequency increases, average power dissipation is increased, but delay decreases significantly. Thus overall power delay product is reduced. We have achieved 44% less PDP on static CMOS inverter based full adder circuit (Fig. 7). It can operate satisfactorily even at higher-frequency ranges due to a minimum PDP.

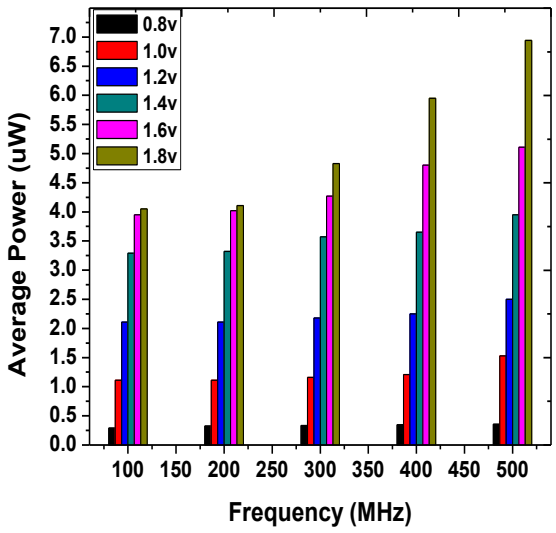

Fig. 7. Average power for different frequency (with different power supply).

C. *Comparison of average power, delay and PDP of different full adder circuit design*

The average power consumption of the proposed full adder is considerably lower than the hybrid full-adder and speed also improved. Another advantage of this circuit is lower requirement of surface. Reduction of average power consumption and propagation delay, PDP of this adder is significantly improved in comparison to the earlier static hybrid full adder Table III; performance measurements of full adder is shown in Table IV.

TABLE III
COMPARISON TABLE
(POWER, DELAY, AND PDP AT 1.8V AND 100 MHZ)

Design	**Average power (µw)**	**Delay (ns)**	**PDP (f j)**	**Transistor count**
C-CMOS	6.2197	0.2921	1.816	28
CPL	7.7198	0.1839	1.420	32
TFA	8.2491	0.2871	2.368	16
TGA	8.4719	0.2939	2.898	20
14T	12.7217	0.3817	4.855	14
10T	14.3449	0.1325	1.902	10
Majority-based	6.3227	0.1854	1.172	NA
Statics COMS inverter FA	5.8459	0.1971	1.152	16
Hybrid	4.1563	0.2240	0.931	16
Proposed FA	**4.0513**	**0.1590**	**0.644**	**16**

TABLE IV
PERFORMANCE SUMMARY (MEASUREMENTS)

Technology	180 nm CMOS
Circuits design scheme	MTVL
CMOS transistor count	16
Average Power Consumption at 1.8V, 100MHz operating frequency	4.0513 µW
Power delay product at 1.8V 100MHz operating frequency	0.6440 f j
Chip Area	8.52 µm x 7.38µm

V. CONCLUSIONS

It is a challenging task to keep total output voltage swing and delay minimization in low power VLSI circuits due to output voltage degradation. Many design techniques exist focusing on the reduction of leakage current and performance improvement at low biasing voltage, etc. A new MTVL modified 16T double gate 1-bit full adder proposed in this paper design techniques is most suitable for controlling leakage current and also reducing power consumption, PDP and area. The output waveform and average power are simulated using SPICE at power supply ranging from 0.8V to 1.8V and frequency range 100MHz to 500MHz. Low power high-speed double gate 16T 1-bit full adder structure is suitable for low-value Vdd as well as low average power and application of this circuit to build a low-power high-performance VLSI system.

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