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Application of Neural Network for Testing Selected Specification Parameters of Voltage-Controlled Oscillator

Damian Grzechca and Sebastian Temich

***Abstract*—In this paper, the application of the Artificial Neural Network (ANN) algorithm has been used for testing selected specification parameters of voltage-controlled oscillator. Today, mixed electronic circuits specification time is an issue. An analog part of Phase Locked Loop is a voltage-controlled oscillator, which is very sensitive to variation of the technology process. Fault model for the integrated circuit voltage control oscillator (VCO) in ring topology is introduced and the before test stage classificatory is designed. In order to reduce testing time and keep the specification accuracy (approximation) on the high level, an artificial neural network has been applied. The features selection process and output coding for specification parameters are described. A number of different ANN have been designed and then compared with real specification of the VCO. The results obtained gives response in short time with high enough accuracy.**

***Keywords*—Specification driven testing, voltage-controlled oscillator, ring oscillator, artificial neural network.**

I. Introduction

ANALOG and mixed signal integrated circuit testing has gained wide attention of researchers in a testing area. The additional problem is associated with modern fabrication process: limited number of nodes for measurement and number of fault free elements scattered within their tolerance ranges[1].

Due to the problem, integrated circuits are tested several times. The first test is performed before packaging at wafer level to identify instabilities in the fabrication process. Finally built module are tests after packaging to verify the actual design specifications [2].

In order to speed up the product testing procedure to short time-to-market time, the simulation before test stage (SBT) is introduced. SBT using software for computer analysis of electronic circuits allows simulating most of the damage that may occur at the production stage and their impact to the specification parameters (i.e. changing the length and width of the transistor channel as a result of photolithographic mask displacement, etc.). Using all simulated damages, the damage dictionary is created and use at the circuit testing stage [3], [4].

Among the test algorithms, the most attention is focused on the heuristic methods, evolutionary techniques, fuzzy logic, support vector machines, artificial neural networks [5]–[7].

This paper presents the use of artificial neural networks to short testing time of VCO selected specification parameters. In the testing process (Fig. 1), the output signal of the generator is analyzed and characteristic features are measured. Measured features become input parameters of the neural network. Based on the features, the learned neural network indicates (with the believe factor value – see sec. 3), which of the design specification parameters are within the tolerance limits.

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First Author and Second Author are with Institute of Electronics, Silesian University of Technology, Poland (email: dgrzechca@polsl.pl, stemich@polsl.pl).

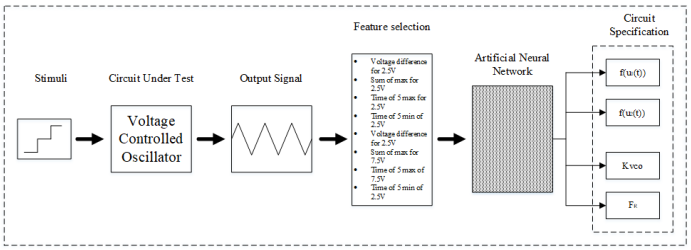

Fig 1. Testing procedure.

II. Circuit under test

A. Voltage-Controlled Oscillator

A voltage-controlled oscillator (VCO) is one of the most important blocks in analog and digital electronics [8]. It is main functional block in phase-locked loops systems, or as a clock generator in clock generator circuits [8].

Voltage-controlled oscillator may be implemented by several solutions: ring oscillator topology, LC-oscillator topology, current starve topology, etc. [8], [9]. Ring oscillator is a cascaded combination of delay stages, connected in a close loop. The ring oscillator designed with a loop of delay stages has many advantages: It needs lower voltage to achieve oscillations, has low power consumptions for high frequencies and provides wide tuning range.

VCO, considered as circuit under test (CUT) is based on a current starves topology, which is similar to ring oscillator topology. The two stages current-starved VCO is presented in Fig.2.

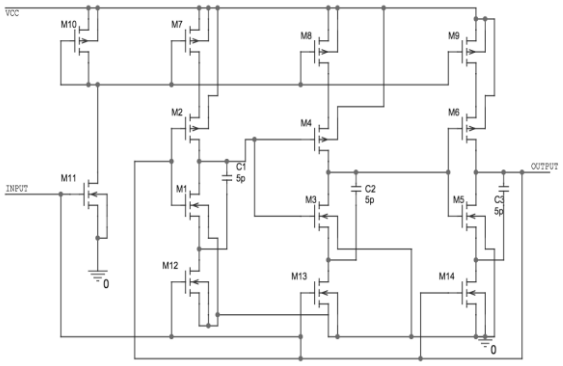

Fig 2. Two stages current-starved VCO.

Transistor M1 (NMOS) with M2 (PMOS) operates as inverter, while M7 and M12 operate as current sources. These 4 transistors form one structure of the oscillator. This structure is repeated once again by M3- M14 transistors, creating a 3-step ring of the oscillator [8].

B. Functional parameters of voltage-controlled oscillator

VCO functional test should be directed on measurement of at least 3 different characteristic of output signal. Selected functional parameters have effect on quality of produced VCO. Due to the structural errors, at the testing stage, functional test of CUT should contain:

- Frequency tuning characteristic ($f(V)$), expresses the relationship between a VCO operating frequency at the tuning voltage applied [9],
- Output power (P_{dBm}), measured into a 50Ω load [2],
- Phase noise (P_N in dBc/Hz), which describe single sideband phase noise of the oscillator. It is composed of noise close to the flicker noise and noise measured at a spacing of constant value [2],
- VCO gain (K_{VCO}), measured in (Hz/V), which describes change in frequency value due to change in the input signal voltage [2],
- Frequency tuning range (f_R), is a difference between maximum and minimum output signal frequency value [2],
- Lock time (T_{Lock}), is a time after which the output frequency is stabilized (at the desired level)[8].

It is important that the frequency of the designed generator for applied voltage is in the desire range, therefore a circuit testing process starts with frequency measurement (f_2, f_1) for two different testing voltage signals (u_{in}^1, u_{in}^2). The output frequencies for the input signals should be within specification range of the circuit, expressed as (1). Also, in fault free VCO, frequency changes in function of input voltage signal are represented by linear function. With frequency change function, VCO gain is related. VCO gain enumerates changes in frequency per unit of tuning voltage change (2).

$$f_R = f_2 - f_1 \tag{1}$$

where f_2 is a frequency corresponds with u_{in}^2 and f_1 is a frequency corresponds with u_{in}^1.

$$K_{VCO} = \frac{f_2 - f_1}{u_{in}^2 - u_{in}^1} \tag{2}$$

In order to correctly determine the frequency of the output signal, it is necessary to determine the T_{lock} time after which the frequency difference of consecutive periods is less than 1%. For the analyzed circuit the frequency stabilization is achieved after 9 signal periods (4.6 ms).

This paper is focused on specification test where for each transistor parametric fault, four specification parameters are checked - f_1, f_2, f_R, K_{VCO}. The tested circuit pass the specification test if following parameters are in range: $f(u_{in}^1) \in$<6.9; 7.28>kHz, $f(u_{in}^2) \in$ <7.46; 7.76>kHz, $f_R \in$ < 1.04; 1.09>, $K_{VCO} \in$ < 98; 101>.

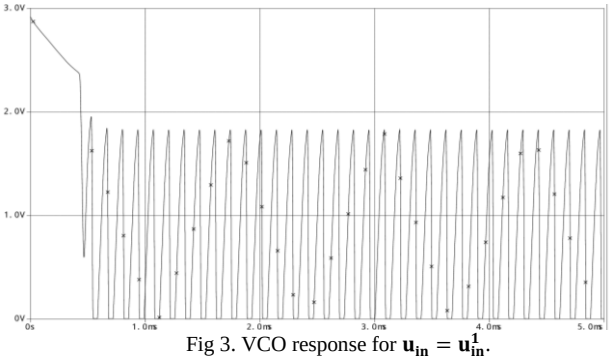

Fig 3. VCO response for $\mathbf{u_{in}} = \mathbf{u_{in}^1}$.

C. Fault models

Due to the Fig.2, presented voltage-controlled oscillator is based on NMOS and PMOS transistors. In technological process, transistor errors are results of i.e. photolithographic mask deviations or technological aspects errors. This group of errors has influence on parametric values of transistor structure: length, width or oxide thickness. Changing the values of these parameters has a direct influence on the parameters of the VCO's design specifications.

Using PSpice simulation software, fabrication process of used transistors is modeled by length (L), width (W) and oxide thickness (T_{OX}).

Nominal values of PMOS (P) and NMOS (N) transistors are defined as:

$$\boldsymbol{L_{nom}^P},\ \boldsymbol{L_{nom}^N},\ \boldsymbol{W_{nom}^P},\ \boldsymbol{W_{nom}^N},\boldsymbol{T_{OXnom}^P},\ \boldsymbol{T_{OXnom}^N}$$

The maximum range for parameters L, W, T_{OX} has been set to:

$$\boldsymbol{L}^{P/N} \in \langle \mathrm{L}_{\mathrm{nom}}^{\mathrm{P/N}}; L_{max}^{P/N} \rangle, \boldsymbol{L}^{P/N} \in \langle L_{min}^{P/N}; \mathrm{L}_{\mathrm{nom}}^{\mathrm{P/N}} \rangle$$

$$\boldsymbol{W}^{P/N} \in \langle \mathrm{W}_{\mathrm{nom}}^{\mathrm{P/N}}; W_{max}^{P/N} \rangle, \boldsymbol{W}^{P/N} \in \langle W_{min}^{P/N}; \mathrm{W}_{\mathrm{nom}}^{\mathrm{P/N}} \rangle$$

$$\boldsymbol{T_{OX}^{P/N}} \in \langle \mathrm{T}_{\mathrm{OXnom}}^{\mathrm{P/N}}; T_{OXmax}^{P} \rangle, \boldsymbol{T_{OX}^{P/N}} \in \langle T_{OXmin}^{P/N}; \mathrm{T}_{\mathrm{OXnom}}^{\mathrm{P/N}} \rangle$$

The tolerance range for simulation has been set to:

$$t_L^P, t_L^N, t_W^P, t_W^N, t_{T_{OX}}^P, t_{T_{OX}}^N$$

Transistor nominal behavior is represented by the following ranges:

$$\mathrm{L}_{\mathrm{nom}}^{\mathrm{P/N}} \in \langle \mathrm{L}_{\mathrm{nom}}^{\mathrm{P/N}} - \mathrm{t}_{\mathrm{L}}^{\mathrm{P/N}}; \mathrm{L}_{\mathrm{nom}}^{\mathrm{P/N}} + \mathrm{t}_{\mathrm{L}}^{\mathrm{P/N}} \rangle$$

$$\mathrm{W}_{\mathrm{nom}}^{\mathrm{P/N}} \in \langle \mathrm{W}_{\mathrm{nom}}^{\mathrm{P/N}} - \mathrm{t}_{\mathrm{W}}^{\mathrm{P/N}}; \mathrm{W}_{\mathrm{nom}}^{\mathrm{P/N}} + \mathrm{t}_{\mathrm{W}}^{\mathrm{P/N}} \rangle$$

$$\mathrm{T}_{\mathrm{OXnom}}^{\mathrm{P/N}} \in \langle \mathrm{T}_{\mathrm{OXnom}}^{\mathrm{P/N}} - \mathrm{t}_{\mathrm{T_{OX}}}^{\mathrm{P/N}}; \mathrm{T}_{\mathrm{OXnom}}^{\mathrm{P/N}} + \mathrm{t}_{\mathrm{T_{OX}}}^{\mathrm{P/N}} \rangle$$

In order to increase of the statistical analysis, parametric damage of the model was divided into X number subranges. Assuming the X parameter as length, width or oxide thickness and $\mathrm{X}^{\mathrm{nom}}$ as nominal value, the new subrange middle value $\mathrm{X}^{\mathrm{mid}}$ is presented as:

$$\mathrm{X}_{\mathrm{i}}^{\mathrm{mid}} = \mathrm{X}_{\mathrm{i}}^{\mathrm{nom}} \cdot \mathrm{t}_{\mathrm{i}}$$

where $\mathrm{t}_{\mathrm{i}} \in \{0.7, 0.75, 0.8, 0.85, 0.9, 0.92, 0.94, 0.96, 0.98, \ldots$

$0.99, 0.992, 0.9940.996, 0.998, 1, 1.002, 1.004,$

$1.006, 1.008, 1.01, 1.02, 1.04, 1.06, 1.08 \ \ldots$

$1.1, 1.15, 1.25, 1.30\}$

Each range is defined as follows:

$$X_i^{mid} \in \langle X_i^{nom} \cdot t_i - tol_i; X_i^{nom} \cdot t_i + tol_i \rangle$$

where tol_i is tolerance parameter.

A number of Monte Carlo analyses within predefined ranges have been set to S with uniform distribution (e.g. S = 50).

D. Circuit under test simulation profile

The artificial neural networks proposed in this paper are aimed checking specification parameters in case of parametric faults in NMOS and PMOS transistors. Transistor nominal parameters (Fig.1) was set to: $\boldsymbol{L}_{nom}^{N} = 6.25\mu\text{m}$, $\boldsymbol{L}_{nom}^{P} = 25\mu\text{m}$, $\boldsymbol{T}_{OXnom}^{N} = 2\mu\text{m}$, $\boldsymbol{W}_{nom}^{N} = 3\ \mu\text{m}$, $\boldsymbol{T}_{OXnom}^{P} = 2\mu\text{m}$, $\boldsymbol{W}_{nom}^{P} = 6.25\mu\text{m}$. Tolerance for each simulation was set:

$$tol_{L,W,T_{OX}}^{N/P} = 0.1\% \rightarrow t_i \in < 0.99, 1.01 >$$
$$tol_{L,W,T_{OX}}^{N/P} = 1\% \ \textit{for the rest of the } t_i$$

For each simulated set, *S* = 150 Monte Carlo analysis was generated.

At the simulation stage, two step functions has been considered: $u_{in}^1 = u_{in}^1 \cdot 1(t)$ and $u_{in}^2 = u_{in}^2 \cdot 1(t)$, where $u_{in}^1 = 2.5\text{V}$ and $u_{in}^2 = 7.5\text{V}$, for both rising, time was equal - $time_{rise} = 0.7\text{ms}$. The exemplary response for transistor nominal values and $u_{in} = u_{in}^1$ is presented in Fig. 3.

E. Output signal feature selection

The main goal of the presented paper is to short the test time with compare artificial neural networks in order to increase detection accuracy. For this purpose output signal was analyzed and for both input stimuli (u_{in}^1 and u_{in}^2), output signal was decimated. The following samples were determined for each period:

1. Maximum value of each period $u_{M_p}^{1/2}$,
   where p is the value of the appropriate maximum.
   The maximum value of each period is determined with (3).

$$\frac{\partial u_{out}^{1/2}}{\partial t} < 0 \tag{3}$$

2. The first minimum $u_{L_p}^{1/2}$ before $u_{M_p}^{1/2}$, according to (4),
3. The first minimum $u_{R_p}^{1/2}$ after $u_{M_p}^{1/2}$, according to (4),

$$\frac{\partial u_{out}^{1/2}}{\partial t} > 0 \tag{4}$$

According to the assumptions of test time shortening for the CUT, the proposed testing method should analyze circuit response shorter than the time needed to reach the T_{Lock} ($T_{test} < T_{Lock}$)

Samples of the $u_{out}^{1/2}$ from u_{in}^1 and u_{in}^2 of the CUT are forming into an input vector N_{imp}, which is applied to the input of each artificial neural network. The length of the N_{imp} depends on the number of analyzed periods, i.e. for 2 periods, the input vector N_{imp}:

$$N_{imp} = [v_1, v_2, v_3, v_4, v_5, v_6, v_7, v_8, v_9, v_{10}] =$$
$$= [u_{L_1}^1, u_{M_1}^1, u_{R_1}^1, u_{M_2}^1, u_{R_2}^1, u_{L_1}^2, u_{M_1}^2, u_{R_1}^2, u_{M_2}^2, u_{R_2}^2]$$

III. Artificial Neural Networks

Development of a good artificial neural network model depends on several coefficients. The first coefficient is related with used data, the second describes model structure or network architecture, next factor is a model complexity and size. Finally quality of the network is strongly depended on training. Training an artificial neural network contains updating the weights to minimize the error between the outputs and the actual response [10].

A. Artificial Neural Network structure

In the presented research an artificial neural networks (ANN) have been used with CUT output signal samples to check selected specification parameters of VCO ($f(u_{in}^1)$, $f(u_{in}^2)$, K_{VCO}, f_R). Following ANN is described as:

$$ANN = \{in, l, out\} \tag{5}$$

where *in* is the number of ANN inputs, *out* is the number of ANN outputs and:
$l = \{l_a = 1, \ldots, N\}$

$$l = \{l_a = 1, \ldots, N\} \tag{6}$$

where l_a is the number of neurons in an *a-th* layer.
The number of ANN inputs (*in*) depends on the number of $u_{out}^{1/2}$ samples (see 2.5) and is equal N_{imp}. Following neural networks have 1 hidden layer and number of neurons (l_1) belongs to:

$$l_1 \in < 1; n_m > \tag{7}$$

Introducing a limit on the number of neurons occurring per one input of 3. The maximum number of neurons in the hidden layer is equal $n_n = N_{imp}{}^3$.
According to assumptions, the constructed neural network should indicate on the basis of the inputs, which of the selected CUT design specifications is fulfilled. For voltage-controlled oscillator, each specification can be described with 0 and 1, where 0 encodes missing of the selected specification and 1 represents fulfillment the selected specification. Dividing all measured specifications into 0 and 1 groups. Taking into account the measured specification parameters of the CUT, the output of the neural network is a binary function 1 from N, where N is the number of all possible combinations (N = 16).

$$out = \begin{Bmatrix} 1111, \text{where all the selected specification} \\ \text{parameters are correct} \\ .... \\ 0\,0\,0\,0, \text{where none of selected specification} \\ \text{parameters are correct} \end{Bmatrix}$$

The first bit corresponds with specification of a $f(u_{in}^1)$, the second corresponds with specification of a $f(u_{in}^2)$, the third bit corresponds with specification of a f_R parameter and the last bit corresponds with a specification of a K_{VCO} parameter.

Each neuron in the hidden layer is described by the activation function for calculating the output of each neuron [11]. In the learning process Broyden-Fletcher-Goldfarb-Shanno algorithm were used [10].

B. *Artificial Neural Networks testing stage*

In the learning process for each N_{imp}, artificial neural networks with different number of neurons (from set of l_1) in the hidden layer and different activating functions of neurons in hidden and output layer, were generate to the research problem.

To estimate the accuracy of the obtained model, artificial neural network has been trained on a measured set of inputs and corresponding outputs (Fig.4). Training algorithm provides minimization of difference between measured output values designated outputs. On a predefined training data set $\hat{y}_i$

$$\hat{y}_i \to y_i, for\ i = 1 \dots N_T$$

where N_T is the size of training set.

To calculate the accuracy of build neural networks two functions: cross entropy - E_{CE} (8) and sum of squares - E_{SOS} (9) were used:

$$E_{SOS} = \sum_{i=1}^{N} (y_i - \hat{y}_i)^2 \tag{8}$$

$$E_{CE} = -\sum_{i=1}^{N} \hat{y}_i \ln\left(\frac{y_i}{\hat{y}_i}\right) \tag{9}$$

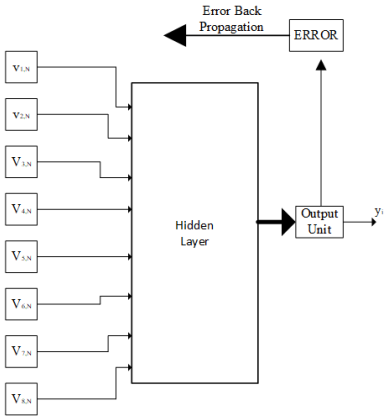

Fig 4. Learning diagram.

In the validation process, all generated artificial neural networks have been compared in terms of the classification efficiency and the one with the highest efficiency was chosen. Table I presents efficiencies for all periods of outputs signal.

Comparing the efficiency of classification in the validation process, it can be seen that the most effective is use of 4 periods of output signal. The time needed to extract samples from 4 periods is t_p = 2.2 ms and is 2 times shorter than the time necessary to reach T_{Lock} of CUT. This case was chosen as the best one for analyzed problem and is discussed in the following.

IV. Selected Artificial Neural Network

According to above, the best classification efficiency was reached for 4 periods of $u_{out}^{1/2}$ with artificial neural network constructed as multilayer perceptron with 228 neurons in hidden layer. Neurons in hidden layer are active with tanh function and output neurons are activate with softmax function [11]. The highest classification efficiency was reached after 352 epochs.

A. *Trust coefficient*

Lean on the value of activation function of neurons in the output layer, the studied CUT based on the input vector N_{imp} is assigned to one of the classes. The neurons in output layer based on the activation function can take different values. Information of the value of activation function can be used to introduce the classification trust coefficient-T_c (10). This coefficient informs at the testing stage, how credible is the CUT classification.

$$T_C = (1 - (1 - f_a(z))) \cdot 100 \tag{10}$$

TABLE I
COMPARISON OF ARTIFICIAL NEURAL NETWORKS FOR 8 PERIODS OF CUT OUTPUT SIGNAL

Number of Periods	Learning efficiency (%)	Validation efficiency (%)	Overall efficiency (%)	Epochs	AFIHL[b]	AFIOL[c]	Error function
1 period	73.46	73.75	73.39	186	Tanh	Softmax	Entropy
2 periods	87.64	85.83	86.35	292	Logistic	Softmax	Entropy
3 periods	88.83	85.59	86.65	326	Tanh	Softmax	Entropy
4 periods	90.98	85.77	87.74	352	Tanh	Softmax	Entropy
5 periods	88.35	85.29	86.19	202	Logistic	Softmax	Entropy
6 periods	87.89	84.70	85.80	206	Logistic	Softmax	Entropy
7 periods	87.28	84.64	85.78	503	Exponential	Tanh	SOS
8 periods	87.52	84.82	86.21	504	Tanh	Tanh	SOS

[b] *AFIHL* – activation function of neurons in hidden layer;
[c] *AFIOL* – activation function of neurons in output layer.

where $f(x)$ is a value of activation function of output layer.

Although the CUT is classified into one of the classes, the tester has the ability to check how good the classification result is.

Adapting to the binary response structure of the artificial neural network, the value of T_c is also represented in binary form. Binary representation of the artificial neural network output allows implementation of ANN in microcontroller structure where the total response takes only 2, 8-bit registers of the μC.

Taking into account the classification process and the value of the T_c coefficient, the final structure of the constructed artificial neural network is as on Fig. 5.

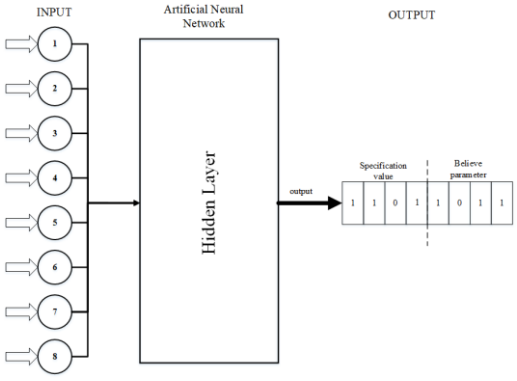

Fig 5. Artificial neural network structure with binary output of CUT classification and classification trust coefficient.

B. Comparison with Support Vector Machine

The selected artificial neural network was compared with another widely used data classification technique- Support Vector Machine[12]. Similarly to artificial neural network, input vector N_{imp} was used and assignation is to 16 classes. Support Vector Machine used for comparison has radial kernel function (11).

$$\phi = \exp(-\gamma \left| c_i - c_j \right|^2) \qquad (11)$$

where $\gamma = 0.056$, c_i and c_j are variables.

Additional comparison SVM with ANN is presented in Table II.

TABLE II
EFFICIENCY OF SVM AND ANN

Classification method	Efficiency (%)
Support Vector Machine	74.42
Artificial Neural Network 18-228-16[1]	87.74

[1] Artificial Neural Network a-b-c: a- inputs, b- number of neurons in a hidden layer, c-output possibilities.

V. CONCLUSION

The paper presents application of artificial neural network to shorten test time (maintaining high classification efficiency) of a design specification of a voltage-controlled oscillator associated with damage occurring at a production stage that affects the technological parameters of the applied transistors. To perform a design test, the CUT response was decimated. Based on the selected samples, the neural network determines the correctness of the chosen parameters of the design specification of the studied circuit. The proposed diagnostic method also informs the tester about the neural network's accuracy with proposed T_c coefficient.

A constructed artificial neural network classifier was compared with support vector machine with radial kernel function classifier. As it can be seen, constructed artificial neural network has much higher classification efficiency than support vector machine. The short time (t_p) of output signal feature extraction, simplicity of generating the features as well as the easy construction of artificial neural network makes the proposed method successfully adapted for other IC.

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