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A Systematic Approach to Determining the Duty Cycle for Regenerative Comparator Used in WSN

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***Abstract*—A low power regenerative comparator is very useful in Successive Approximation Register (SAR) type Analog to Digital Converter (ADC) for a Wireless Sensor Node (WSN). A regenerative type comparator generates output pulses by comparing input with a reference input. This paper deals with control of a power with an adjustable duty cycle. The regenerative comparator with an adjustable duty cycle and a positive feedback of a latch will help in improving accuracy, speed and also in achieving the less power consumption. The optimum value of a duty cycle is determined with metastability timing constraints. The proposed low power regenerative comparator circuit is designed and simulated by using TSMC 180 nm CMOS technology. The comparator consumes power as low as 298.54 nW with a regenerative time 264 ps at 1 V power supply.**

***Keywords*—SAR, ADC, WSN, regenerative comparator, metastability**

I. Introduction

ONE of the power consuming component in WSN is comparator [1]. Many researcher have derived low power comparator for WSN [2] − [4] . All these techniques though leading to low power consumption they may be time consuming because of random choice of duty cycle. To have an energy-limited use in wireless sensor networks require a low power comparator logic for ADC to extend the product life [5] − [7].

In [8], a dynamic comparator is more accurate due to modified digital foreground technique that uses a small size transistor which leads to less non-linearity in switching capacitor array. The auxiliary capacitor array and digital foreground technique are used to generate comparison levels due to which this technique will consume more power and leads to less speed. The dynamic latch comparator used in [9] has low power consumption, and it is more accurate due to the common mode voltage kept at mid-rail voltage value. Therefore, the comparator offset appears as a static offset. This offset does not affect accuracy, but the input voltage range decreases. Due to a decrease in the input differential voltage, the regeneration time goes towards infinity causing less speed. In [10], a two-stage dynamic comparator with the first stage as an amplifier and second stage as a latch. This dynamic logic reduces the significant amount of power due to lower sampling rate 1 KS/s. The monotonic switching sequence used in [10] will induce a dynamic offset due to charge injection of a capacitor, and therefore the accuracy and speed are getting affected. All these techniques have either low power consumption or more precision with less speed. None of these techniques have achieved all three parameters i.e. low power, high speed, and more accuracy simultaneously. This paper deals with systematic approach to determining optimum duty cycle for deriving high speed, low power regenerative comparator.

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II. Methodology

The duty cycle has a direct relationship with the average power consumed. A comparator uses a clock signal, i.e., variation in the period of a clock varies the power. The optimum duty cycle defined as the ratio of the active or on-period to the total pulse width. The non-linear behavior of timing constraints (T_S, T_H) i.e. setup and hold time will affect the power consumption. The optimum time is determined using minimum and maximum T_S, T_H. This timing constraint will insert additional stages of a register and dissipating extra power. Therefore, to determine the appropriate timing constraints for a valid range is considered i.e. ($T_{\mathrm{S,r}}$, $T_{\mathrm{H,r}}$)

III. SAR ADC

As wireless sensor node is a battery operated node and most of the time it is in the sleep mode. When there is an activity in the vicinity of a node, it will wake-up. Next, to the processor, the ADC will consume more power. So to save energy in the wireless node, an ultra-low power comparator part of a SAR ADC is proposed. The conventional architecture [5] of a SAR type ADC has demonstrated in Fig. 1. It has three entities namely a comparator, SAR logic either synchronous, asynchronous or mixed mode and current or voltage mode type DAC. The comparator performs the comparison of analog input with the reference signal coming from DAC. The comparator output generates square pulses. A SAR logic shifts and counts these pulses. The DAC is converting back digital pulses to the analog reference signal of a comparator. The critical time (T_{critical}) is the worst case delay for one-bit conversion shown in Eq. (1), and defined as the summation of comparator time, SAR logic, and conversion time of a DAC. Where the comparator time (t_{comp}) is the minimum cycle time required to convert the input signal into pulses. The SAR logic time (t_{logic}) is the conversion time to count these pulses using SAR logic, and the time required to complete its conversion from digital to analog is express as DAC time (t_{DAC}). The simplified version of critical time has found using Eq. (2).

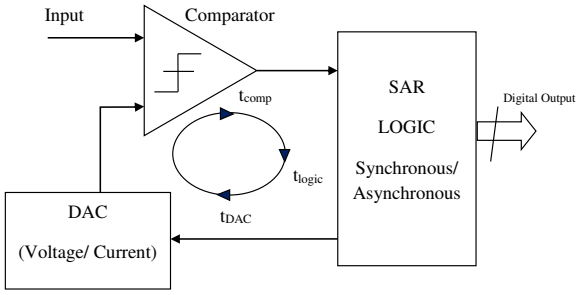

Fig. 1. Conventional SAR ADC architecture [5, Modified]

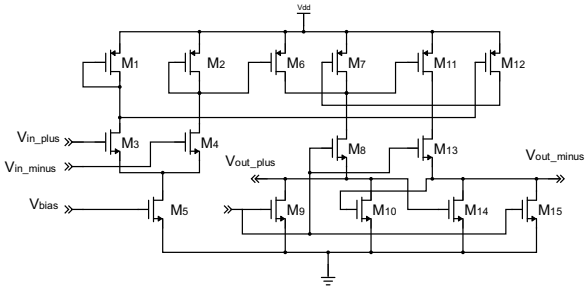

Fig. 2. Schematic View of CMOS Dynamic Comparator

$$T_{\text{critical}} = t_{\text{comp}} + t_{\text{logic}} + t_{\text{DAC}} \quad (1)$$

$$T_{\text{critical}} = t_{mincycletime} + t_{pd(min)} + t_{DACsettle} \quad (2)$$

The Eq. (1) can rewrite as Eq. (2), concerning the $t_{mincycletime}$ which is the minimum cycle time of a comparatorand $t_{pd(min)}$ is a logical time for conversion from SAR, and $t_{DACsettle}$ is settling time of a DAC respectively .

IV. Regenerative Comparator

The sensor node in the WSN will sense the physical activity with the help of different types of sensors and transducer. This physical phenomenon processed and converted into the digital form and sent it to the base station or server. The basic block of SAR ADC in a WSN is a comparator. The regenerative comparator is showing in Fig. 3. Which has three stages a preamplifier stage-I, preamplifier stage-II, and Latch. The positive feedback latch block used for fast decision with small power and area consumption. The use of the clock pulse can significantly improve comparator performance, speed and low power dissipation with adjustable duty cycle. The clock also eliminates the need for an output buffer which is used in the level shifting the output of the preamplifier stage -II block.

TABLE I
Comparison of Regenerative and Dynamic type comparator

Regenerative Type	Dynamic Type
Sensitivity is high to a small input difference.	Low sensitive
Static power caused by the leakage current and DC current needed for operation.	The Dynamic power associated with charging and discharging of a variable switched capacitor.
Power dissipation is more	Power dissipation is low
High speed	Speed limitation due to the time delay required to charge a capacitor before each comparison.
More accurate	Kickback charge injection causes a significant voltage variation affects the accuracy.

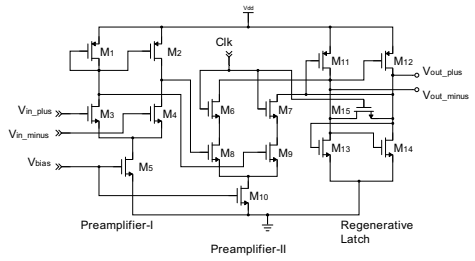

Fig. 3. Schematic View of Proposed CMOS Regenerative Comparator.

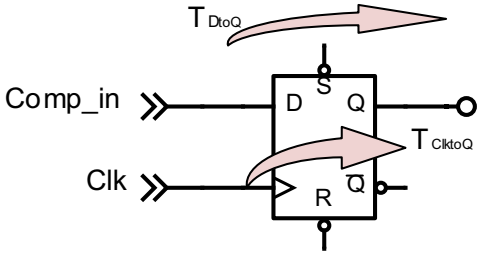

Fig. 4. Block Diagram of D Flip-Flop (SAR Logic)

A. Power control using Duty cycle

Assuming energy; E and power is a rate of change of energy flow per unit time, the peak power, and average power for one full period ($f = \frac{1}{T}$) in terms of energy which are representing in Eq.(3) and Eq. (4).

$$P_{peak} = \frac{E}{\Delta t} \quad (3)$$

$$P_{avg} = \frac{E}{T} \quad (4)$$

The Duty Cycle is the fractional amount of time in which the device is on during any given period is expressing in Eq.(5).

$$Duty - cycle = \frac{\Delta t}{T} \quad (5)$$

Thus, the duty cycle writes as concerning of average and peak power and it is representing in Eq.(6)

$$Duty - cycle = \frac{P_{avg}}{P_{peak}} \quad (6)$$

B. Setup and Hold Time

The SAR logic uses a D-flip-flop structure that is shown in Fig. 4. The input to output delay (T_{DtoQ}) is the signal carrying time to the input of the flip-flop. Time is taken by the flip-flop to get the output when a clock pulse is applied. This is called as a clock to Q delay (T_{ClktoQ}). A width of a clock pulse is too short or long, which will violate the setup (T_S) and

hold time(T_H). These timing parameters are interdependent and also have the non-linear behavior. That is, if hold time is high then setup time is small or vice-versa [11].

C. Optimum Duty Cycle

The duty cycle has a direct relationship with the average power consumed by the circuit shown in Eq. (6). A comparator uses a clock signal, i.e., variation in the period of a clock varies the power. The optimum duty cycle defined as the ratio of the active or on-period to the total pulse width shown in Eq. (7). The non-linear behavior of timing constraints (T_S, T_H) will affect the power consumption. The minimum active period in our case, determined by considering the two scenarios with the worst case condition. The first scenario is ($T_{\mathrm{H,max}}$, $T_{\mathrm{S,min}}$) and second is ($T_{\mathrm{H,max}}$, $T_{\mathrm{S,min}}$). This timing constraint will insert additional stages of a register and dissipating extra power. Therefore, to determine the appropriate timing constraints for a valid range is considered i.e. ($T_{\mathrm{S,r}}$, $T_{\mathrm{H,r}}$) [11] and calculated using Eq. (7). The duty cycle for a valid range is calculated using Eq. (8). The optimum timing constraints is calculated using in Eq. (9) and Eq.(10) respectively for minimum and maximum value of T_S, T_H. The optimum duty cycle is calculated using Eq. (11).

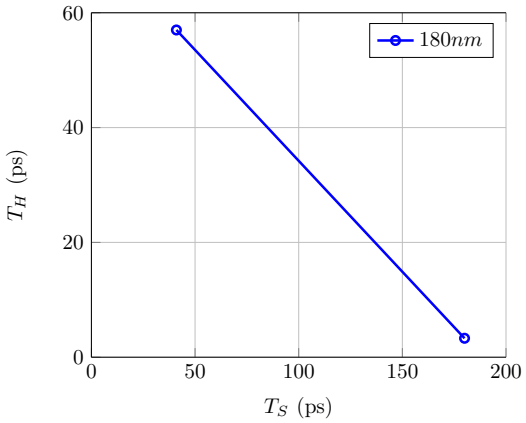

Fig. 5. Interdependent setup-hold time characteristics for 180 nm technology [13]

$$T_{on,r} = T_{DtoQ} + T_{ClktoQ} + T_{S,r} + T_{H,r} \quad (7)$$

$$\omega_r = \frac{T_{on,r}}{T_{total}} \quad (8)$$

$$T_{on,min} = T_{DtoQ} + T_{ClktoQ} + T_{S,min} + T_{H,min} \quad (9)$$

$$T_{on,max} = T_{DtoQ} + T_{ClktoQ} + T_{S,max} + T_{H,max} \quad (10)$$

$$\omega_{optimum} = \frac{T_{on(optimum)}}{T_{total}} \quad (11)$$

Where, $T_{on,r}$ is a on period and ω_r is a duty cycle for a valid range. For 180 nm CMOS Process technology timing parameters are T_S = 41 ps, T_H = 3.3 ps, $T_{S,r}$ = 139 ps, and $T_{H,r}$ = 53.7 ps respectively [11]. The T_S vs. T_H relationship is showing in Fig. 5 and Eq. (12) represents a line [11].

$$T_H = -0.386T_S + 72.839 \quad (12)$$

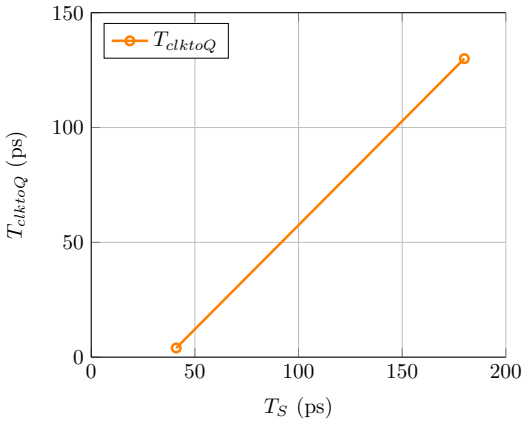

Fig. 6. Interdependent setup-clock to Q time characteristics.

for $41 \leq T_S \leq 180$ in pico-second

$$T_{clktoQ} = T_{clk} - T_S \quad (13)$$

The permissible range (T_{perr}) for T_{clktoQ} is determining as the difference between clock period T_{clk} = 100 ns and set up timing range.

$$T_{perr} = T_{clktoQ,max} - T_{clktoQ,min} \quad (14)$$

$$T_{perr} = 99.95\,\mathrm{ns} - 99.82\,\mathrm{ns}$$

$$= 130\,\mathrm{ps} \quad (15)$$

$$T_{clktoQ} \geq T_H \quad (16)$$

The hold time range is $3.3 \leq T_H \leq 57$ in pico-second , hence it is considering the hold and setup timing condition. The T_S vs. T_{clktoQ} relationship is showing in Fig. 6 and Eq. (17) represents a line,

$$T_{clktoQ} = 0.906T_S - 33.146 \quad (17)$$

Therefore, the range for T_{clktoQ} after considering the permissible range is $4 \leq T_{clktoQ} \leq 130$ in pico-second. The delay between D to Q (T_{DtoQ}) determines T_S vs. T_{clktoQ} range.

$$T_{DtoQ,min} = T_{ClktoQ,min} + T_{\mathrm{S,min}}$$

$$T_{DtoQ,min} = 4\,\mathrm{ps} + 41\,\mathrm{ps}$$

$$= 45\,\mathrm{ps} \quad (18)$$

$$T_{DtoQ,max} = T_{ClktoQ,max} + T_{\mathrm{S,max}}$$

$$T_{DtoQ,max} = 130\,\mathrm{ps} + 180\,\mathrm{ps}$$

$$= 310\,\mathrm{ps} \quad (19)$$

The range for T_{DtoQ} is $45 \leq T_{DtoQ} \leq 310$ in pico-second. Therefore, the duty cycle for a valid range after putting all timing constraints into Eq. (7) and Eq. (8) is,

$$T_{on,r,min} = 45\,\mathrm{ps} + 4\,\mathrm{ps} + 139\,\mathrm{ps} + 53.7\,\mathrm{ps}$$

$$= 241.7\,\mathrm{ps} \quad (20)$$

$$T_{on,r,max} = 310\,\mathrm{ps} + 130\,\mathrm{ps} + 139\,\mathrm{ps} + 53.7\,\mathrm{ps}$$

$$= 632.7\,\mathrm{ps} \quad (21)$$

$$\omega_{r,min}\% = \frac{0.242\,\mathrm{ns}}{100\,\mathrm{ns}}$$

$$= 0.24 \quad (22)$$

$$\omega_{r,max}\% = \frac{0.633\,\text{ns}}{100\,\text{ns}} = 0.63 \quad (23)$$

The optimum value of a duty cycle is calculated after putting all timing constraints into Eq. (9), Eq. (10) and Eq. (11),

$$T_{on,min} = 45\,\text{ps} + 4\,\text{ps} + 41\,\text{ps} + 3.3\,\text{ps} = 93.3\,\text{ps} \quad (24)$$

$$T_{on,max} = 310\,\text{ps} + 130\,\text{ps} + 180\,\text{ps} + 57\,\text{ps} = 677\,\text{ps} \quad (25)$$

$$\omega_{min}\% = \frac{0.0933\,\text{ns}}{100\,\text{ns}} = 0.093 \quad (26)$$

$$\omega_{max}\% = \frac{0.677\,\text{ns}}{100\,\text{ns}} = 0.677 \quad (27)$$

A comparator power has a direct relationship with a duty cycle. The minimum and maximum range of a duty cycle is find out where the power is optimum. Therefore, the optimum region for a regenerative type comparator where minimum power is achieved by varying the duty cycle. A transient simulation result of a regenerative comparator is shown in Fig. 7. The output of a comparator drives the SAR logic which uses a D-flip-flop as a fundamental building block.

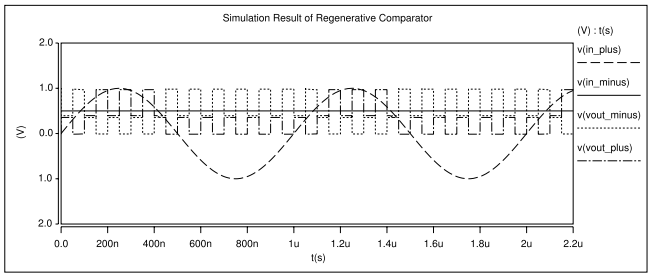

Fig. 7. Transient Simulation of the Regenerative Comparator

D. Calculation of regenerative time (τ) and metastability voltage

The output $\mathrm{V}_1(\mathrm{V}_{outplus})$ and $\mathrm{V}_2(\mathrm{V}_{outminus})$ at an initial voltage and when the switch is closed at a time t = 0 is due to the regenerative amplification properties from the metastable state. Metastability starts at time t_2 and ends at t_3, i.e., resolve time (t_R) is showing in Fig. 8. and representing as Eq. (28). The time τ to exit metastability is expressing in Eq. (29).

$$V_{outplus} = V_{outminus} \exp^{(\frac{t_2 - t_1}{\tau})} \quad (28)$$

$$\tau = \frac{t_2 - t_1}{\ln(\frac{V_{outplus}}{V_{outminus}})} \quad (29)$$

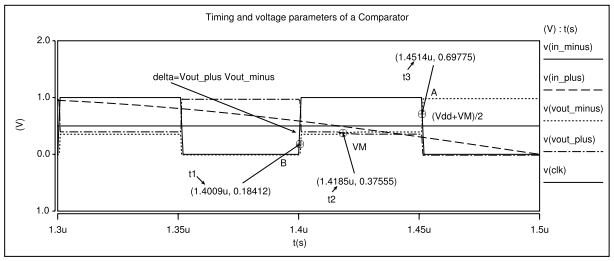

Fig. 8. Simulation Result is showing timing and voltage parameters

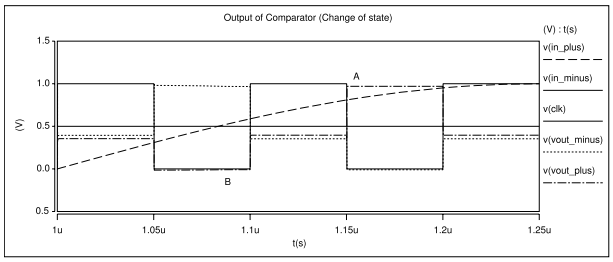

Fig. 9. The output of a comparator(state change) w.r.t clock signal

Using current equations for MOS devices in the regenerative inverters, the metastable voltage (V_M) is write as,

$$I_D = \frac{1}{2}\mu\frac{W}{L}C_{ox}(V_{GS} - V_{th})^2 \quad (30)$$

$$I_{DP} = I_{DN} \quad (31)$$

$$k = \mu\left(\frac{W}{L}\right)C_{ox} \quad (32)$$

$$\frac{1}{2}k_p(V_{DD} - V_{GS} - |V_{thp}|)^2 = \frac{1}{2}k_n(V_{GS} - V_{thn})^2 \quad (33)$$

$$|V_{thp}| = V_{thn} = V_{th} \quad (34)$$

$$V_M = \left(\frac{\sqrt{k_p}V_{DD} + V_{th}\left(\sqrt{k_n} - \sqrt{k_p}\right)}{\sqrt{k_n} + \sqrt{k_p}}\right) \quad (35)$$

The decision time from t_1 to t_3 i.e. t_D is the time to attain a stable digital voltage at the latch output which is expressing in Eq. (36) as a sum of the propagation delay of the latch t_{pd} and time to resolve metastable state t_R.

$$t_D = t_{pd} + t_R \quad (36)$$

From Fig. 8., $t_2(t_D) - t_1(t_{pd})$ = 17.6 ns, $V_{outplus}$ = 0.697 V, $V_{outminus}$ = 0.184 V, τ = 24.69 ns and V_M= 0.4 V.

The output of a regenerative latch shown in Fig. 9., is latched at moment A, the comparator has made its decision because the comparator changes its state. Therefore, no bit error occurs. However, if the latch clocked at moment B, bit error due to the comparator remains in the same state and unable to take a decision. The output of a comparator shown in Fig. 10., have the same value indicating that the comparator has not been able to decide which input has a high or low voltage.

V. Result Discussion

A regenerative type comparator is designed by controlling the duty cycle and finding out the optimum value. The duty cycle cannot change lower than the optimum value otherwise

TABLE II
MEASURED PERFORMANCE SUMMARY AND COMPARISON

Parameters	**[10]**	**[12]**	**[13]**	**This work**	**This work**
Comparator type	Dyna-mic	Dyna-mic	Dyna-mic	Regen-erative (DC=50%)	Regen-erative (DC=10%)
Tech. (nm)	65	130	180	180	180
Supply (V)	1	1	0.6	1	1
Resolution (bit)	8	10	10	10	10
Fsample (MS/s)	50	0.001	0.1	10	10
Power	30.98 µW	2 nW	15 nW	1.28 µW	298.54 nW

DC= Duty Cycle

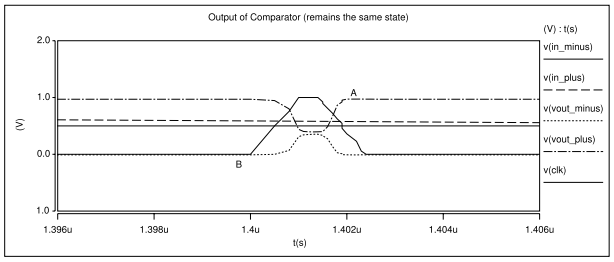

Fig. 10. The output of a comparator(remains the same state) w.r.t clock signal

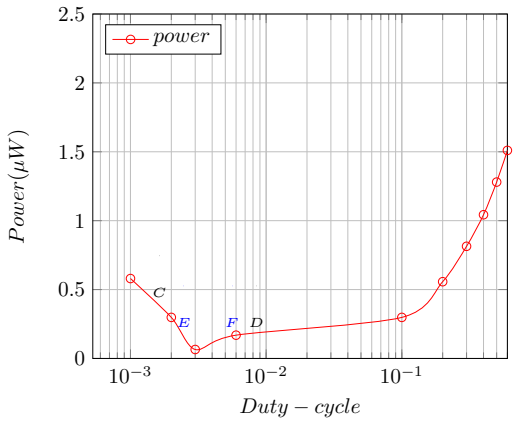

Fig. 11. Duty-cycle Vs Power.

comparator is unable to take a decision. The error in the digital logic affects the performance of ADC which used in WSN. The sampling rate 10 MS/s set with input clock is varying from 50 % to 0.1 % duty cycle at 1 V power supply. In Fig. 11, the range between points C (corresponds to 0.24% duty cycle) to D (corresponds to 0.63% duty cycle) is a valid range and the range between points E (corresponds to 0.1% duty cycle) to F (corresponds to 0.67% duty cycle) is an optimum range. The exponential log-normal plot of a comparator to change its state, shown in Fig. 12., tells how fast it would come out from metastable state voltage (V_M) to a stable digital logic voltage. Ideally, the stable digital logic voltage is half of the sum of a supply voltage. Table II compares the measurement results

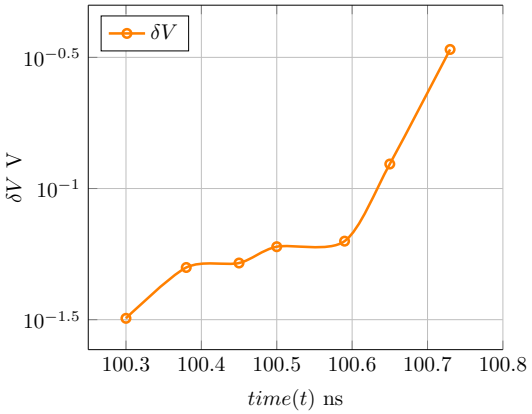

Fig. 12. The Log-normal plot of δV in an exponential region

of this work to previously published comparator used in SAR ADC [10] − [12].

VI. CONCLUSION

A low power regenerative type comparator with adjustable duty cycle for WSN has proposed. Such a comparator consumes 298.54 nW and 1.28 μW power for 10 %, and 50 % duty cycle, respectively at 50 MS/sec. The regenerative time (τ) is 264 ps is achieved using positive feed back of a latch, which lead to increase in speed of operation and accuracy. The proposed comparator is not only leads to an increase in the lifetime of tiny nodes but also improves the overall performance of analog to digital converter used in WSNs.

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