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A 5.5 μW 42nV/$\sqrt{Hz}$ Chopper stabilized Amplifier for Biomedical Application with Input Impedance Enhancement

Ankit Adesara, and Amisha Naik

***Abstract*—The continuous real-time monitoring of diverse physical parameters using biosignals like ECG and EEG requires the biomedical sensors. Such sensor consists of analog front-end unit for which low noise and low power Operational transconductance amplifier (OTA) is essential. In this paper, the novel chopper-stabilized bio-potential amplifier is proposed. The chopper stabilization technique is used to reduce the offset and flicker noise. Further, the OTA is likewise comprised of a method to enhance the input impedance without consuming more power. Also, the ripple reduction technique is used at the output branch of the OTA. The designed amplifier consumes 5.5 μW power with the mid-band gain of 40dB. The pass-band for the designed amplifier is 0.1Hz to 1KHz. The input impedance is likewise boosted with the proposed method. The noise is 42 nV/$\sqrt{Hz}$ with CMRR of 82 dB. All simulations are carried out in 180nm parameters.**

***Keywords*—Biopotential amplifier, input impedance, noise, power, ECG, EEG**

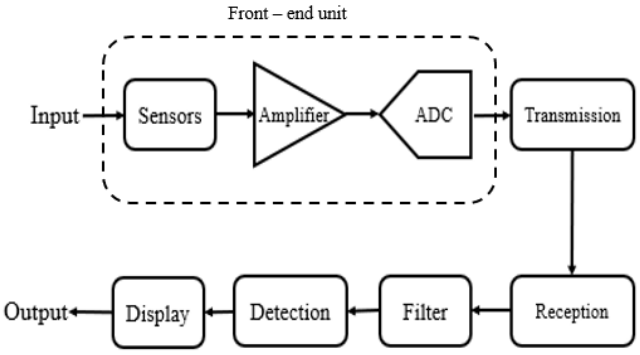

Fig. 1. Block diagram of the acquisition system

I. Introduction

BIOMEDICAL signals consisting of ECG and EEG play a very critical role within the analysis of the different diseases. So, wearable and implantable sensors are extensively used to reveal the physical circumstances for the early detection of cardiovascular diseases. Such bio-medical signals are between 0.1 Hz to 1 KHz with numerous μV to several mV stages of amplitude [1] [2]. Therefore, earlier than digitizing for back end processing, it ought to have been amplified within unique bandwidth to provide proper strength to signal. So, the signal monitoring gadget with the designed amplifier is required.

Signal monitoring is the most vital block in such application as it affords an interface among the sensor and signal processing block as shown in fig.1. It includes the power-hungry analog front-end with operational transconductance amplifier (OTA) [3]. So whilst designing the amplifier, low power consumption is very much crucial to the pre-serve long battery existence of such a device. Further, to realize the robust ECG and EEG indicators, the input-referred noise must beneath in the frequency band. Such bio-signals have low frequency in CMOS technology flicker (or 1/f) noise plays an important role in this design [4]. So, it is very critical to mitigating this issue. From the one of a kind survey [5], it may be said that chopper stabilization approach is well appropriate for flicker noise and DC offset reduction at the side of the OTA in this application. Also, the gain of the amplifier has to have as a minimum of 40 to 60 dB because the amplitude of such signals is very low. Additionally, the parameters like CMRR, offset, output ripple etc. must be taken care while designing [6]. The conventional chopper amplifier is discussed for such application in [7].

Input impedance is also a very important parameter because the electrodes which might be connected with pores and skin have a unique asset. So, the mismatch in the impedance has occurred [8]. So, to mitigate this problem of impedance mismatch, the input impedance of the designed amplifier for the biomedical application need to be greater than 200MΩ.

Here, In upcoming sections, the proposed amplifier is discussed. Also, the technique to enhance the input impedance is likewise discussed and simulated. Apart from this, the noise and offset will be taken care via chopper stabilization method with low power design as the bias current requirement could be very low because of the low bandwidth requirement in the design. Also, the additional block is blanketed to lessen the output ripple inside the recorded signal. At last, the simulation and different analysis with layout design are shown.

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II. Proposed amplifier

The conventional chopper-stabilized bio-potential amplifier offers a lower input impedance and a sizable amount of output ripple [8], Hence, in a traditional block diagram, extra blocks like forward auxiliary path and R-C DC block is proposed as shown in fig.2.

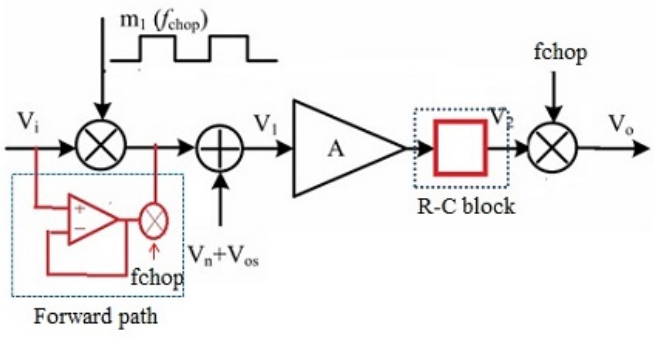

Fig. 2. Basic block diagram of the proposed biopotential amplifier

The forward auxiliary path that is introduced at the input of the amplifier, is changed in a novel manner to boost the input impedance with very much less increment in power dissipation. As a result, the improved model is capable of recording the signal with higher input impedance, low DC offset and reduced ripple on the output at the same time as consuming less power and low flicker noise.

A. Chopper stabilization technique

The fundamental diagram of chopper stabilization technique with an amplifier is shown in fig.3 which represents the different sub-sections like chopper modulator, OTA and low pass filter to perform the necessary operation.

Due to electrochemical reactions at the electrode-tissue interface, the potential difference between two electrodes is generated which needs to be reduced [10]. The low-frequency noise i.e. flicker noise performance can be improved effectively by way of chopper stabilization method which makes it appealing for biomedical application [11]. Also, the design can meet the noise and offset criteria with the aid of the use of this method. In such technique, the OTA offset and low-frequency noise are up-converted by chopper switches to a higher frequency so that by the usage of low pass filter it could be without difficulty filtered out.

B. Enhancement of input impedance

The current state of the art in the acquisition system has successfully met the necessities like power and noise however there is a significant overall performance gap in input impedance [12] [13]. The input branch of OTA is shown in fig.4. For a DC input v_{in}, externally carried out clock signal F_{chop} and input capacitance C_{in}, the input impedance is given by,

$$Z_{in} = \frac{1}{2C_{in}F_{chop}} \tag{1}$$

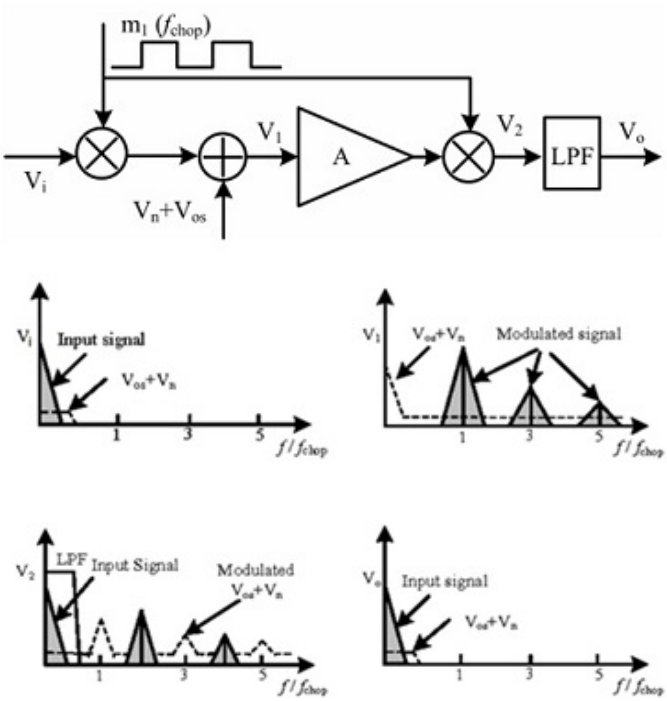

Fig. 3. Chopper stabilization method [9]

Here, the input impedance is maximum of 50MΩ, if C_{in} is considered as 10pF and F_{chop} as 1KHz which is low for the bio-potential amplifier. In fig.4 the DC input current is shown which represents some charge during the period of Δt and therefore there is a finite input current and hence the input impedance is less as well. To reduce the input impedance the input current must be reduced.

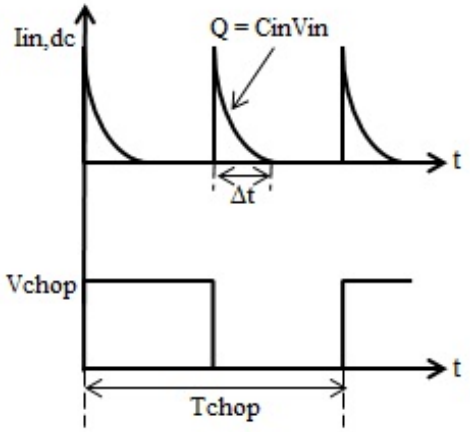

Fig. 4. DC input current

In this design, to enhance the input impedance of the order to at least 200MΩ, another method is used via reduction of DC input current. As shown in fig.5, the alternative forward auxiliary path is introduced to precharge the capacitor such that the potential difference between node n1 and n2 is reduced to zero and hence, Z_{in} is enhanced by way of preserving balance among Cin and F_{chop}.

In fig.5, the changed input branch with the addition of forward-direction is shown. By using such a technique, the

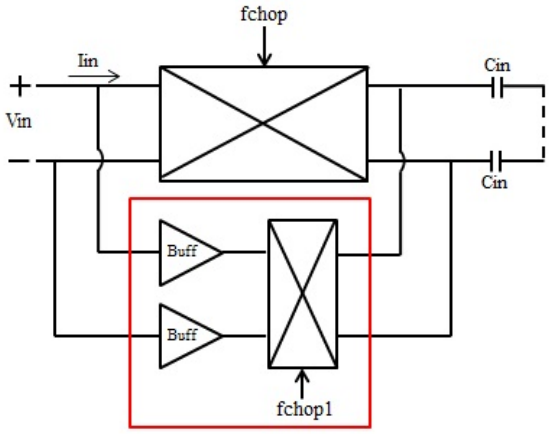

Fig. 5. modified input branch

area is elevated and also power consumption is increased. But through carefully deciding on the bias current of a buffer of the forward path as no longer a good gain and frequency are required, and then increasing the power dissipation is negligible. In this design, the controlled buffer is used within the auxiliary forward path. Here, the method to generate the control signal for the buffer is added in which the precharge phase is defined as shown in fig.6.

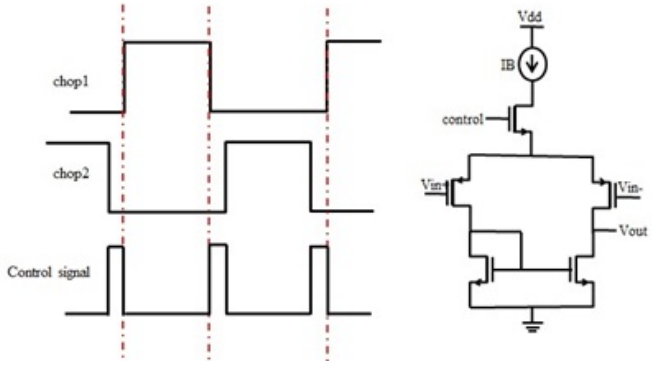

Fig. 6. Control signal waveform with buffer schematic

Also, the buffer is disabled except for the precharge phase. The bias current requirement is decreased and consequently, power is also decreased. The bias current for the forward auxiliary path buffer, for the weak inversion region, is given by,

$$I_{buff} = \frac{8KC_{in}F_{chop}}{25} \tag{2}$$

So, if K=6τ, C_{in} = 10pF and F_{chop} = 1Khz then I_{buff} is given by using eq (2), that's 20nA which is very less, so further, power may be decreased that's used by the forward path and now it could be ignored.

Also, the noise of the buffer which is used in the forward auxiliary path can be analyzed. The noise of the buffer is given by,

$$V_{buff,n}^2 = K_{buff}V_{in,n}^2 \tag{3}$$

Where, K_{buff} is the duty cycle of the control signal. By ensuring the input-referred noise of buffer is much lower than input-referred noise of the OTA, the overall noise of the forward auxiliary path can be negligible but the value ofK_{buff} should be carefully chosen. Here K_{buff} can be derived from [8] by

$$K_{buff} = \frac{KC_{in}}{(25F_{chop})(5I_B)} \tag{4}$$

C. Ripple reduction method

Using chopper stabilization technique with the amplifier, the input-referred DC offset and flicker noise can be reduced however as they're surpassed from chopper modulator once, the noise and offset are up-sampled [14] [15]. Therefore, the ripple on the output of the amplifier is offered which reduces the dynamic range of the amplifier.

In the proposed design, if the output ripple can be modeled as,

$$V_{ripple} = \frac{8V_{off}\omega_m A_m}{\pi g_m R\omega_{chop}} \tag{5}$$

Where K_{buff} is offset voltage, ω_m is the bandwidth of OTA, Am is mid-band gain and ω_{chop} is chopping frequency.

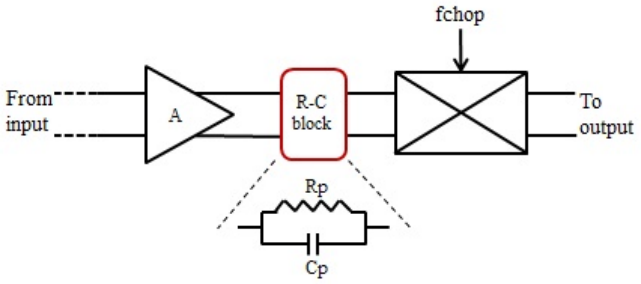

Fig. 7. Ripple reduction method

Here, to reduce the output ripple, the offset current ought to be reduced. To lessen the offset current, the DC block is introduced as shown inside the circuit which consists of the parallel R-C network as shown in fig.7. In this block R_p is considered as larger than the output impedance of the amplifier and C_p is selected such a way that on the F_{chop}, the overall impedance of the DC block is lower than the output impedance of the amplifier so it may be taken into consideration as the short circuit and subsequently the output ripple can be reduced.

D. Specification for the proposed design

In tableI , the specification of the biopotential amplifier is shown as per the current state of art like [1], [2], [8], [16], [15] and from different other researches.

As per that, the specifications of the designed amplifier are finalized for the recording of ECG and EEG signals in biomedical field.

TABLE I
SPECIFICATIONS FOR DESIGN AMPLIFIER

Parameters	Requirements
Process	180nm
Supply	1.8V
Gain	$\geq$ 40dB
Power	$\leq 10\mu$ W
Bandwidth	0.1Hz - 1KHz
CMRR	$\geq$ 80dB
Noise	$\leq 60nV/\sqrt{Hz}$

In the following section, the implementation as per specifications and the results from the different analysis are discussed.

III. IMPLEMENTATION AND RESULTS

In fig.8, the schematic diagram of the proposed amplifier is shown wherein which the forward auxiliary path with the control block and R-C impedance circuits i.e. DC block are added to enhance input impedance and decrease ripple respectively

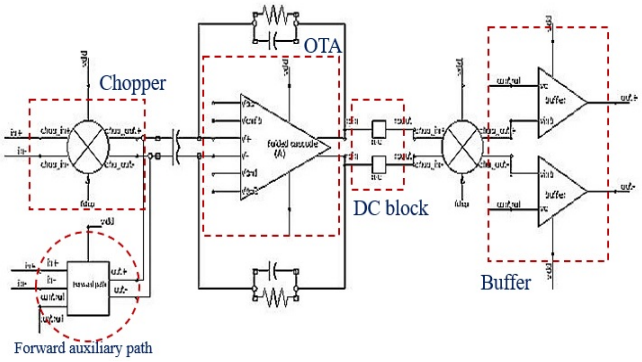

Fig. 8. Schematic diagram of the proposed biopotential amplifier

As shown in the schematic diagram, the various subblocks are included to create an overall front-end biopotential amplifier along with chopper, folded cascode OTA, buffer, forward path and R-C impedance network. From the following subsection, the implementation and simulation of every block are discussed.

A. Operational Transconductance Amplifier

The OTA is the principal building block of the designed amplifier. Here, the folded cascode OTA is designed to achieve required gain, large swing for input with fewer amplitudes and high output impedance so that there is no need of the extra low pass filter at output side and thus, the overall power consumption can be reduced. In fig.9, the schematic of the OTA is shown.

With this OTA, the common-mode feedback (CMFB) circuit that is used to adjust the common-mode output level for double-ended OTA and biasing circuit which requires to make transistor works in proper operating region i.e. saturation region for a given amplifier are shown in fig.10.

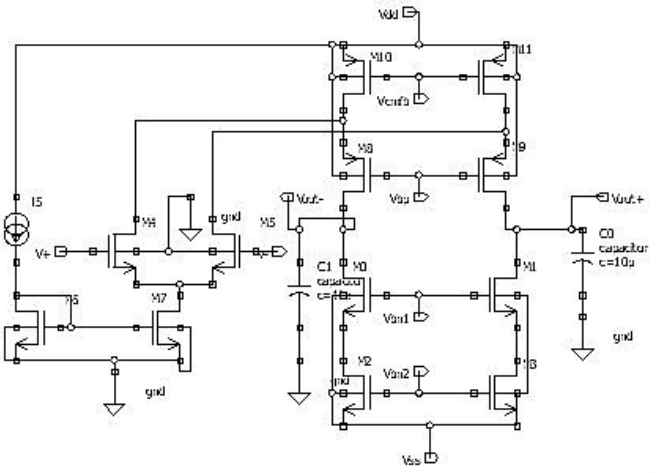

Fig. 9. Folded cascode OTA

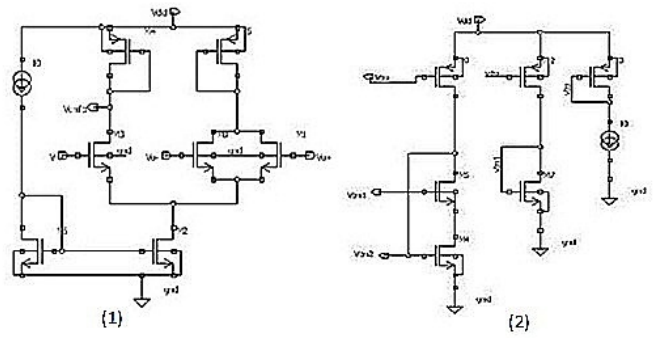

Fig. 10. (1) CMFB circuit and (2) Biasing circuit

B. Chopper and clock generator

The four nMOS switches are used to implement the chopper modulator as shown fig.11. To manage the nMOS switches, the clock generator circuit is used to generate two non-overlapping clocks. Also, the transient analysis of both the sub blocks is shown.

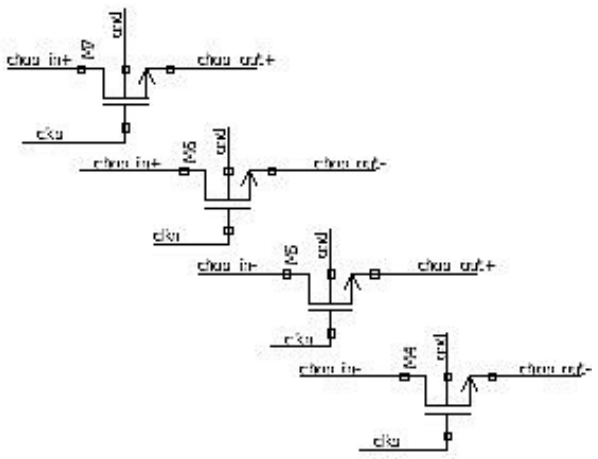

Fig. 11. Chopper modulator

In fig.12, the transient analysis of chopper modulator is shown in which the modulated wavform is generated for a specific input.

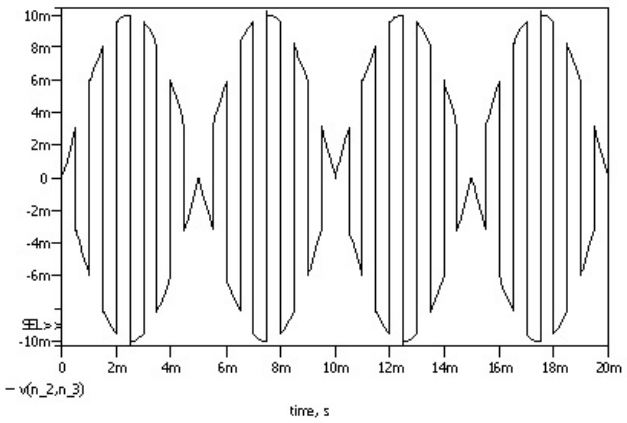

Fig. 12. Modulated waveform

The chopping frequency is taken into consideration as the upper frequency of OTA which is 1KHz in this design for the right operation. As shown in fig.13, the clock generator circuit is designed by NAND gate and an inverter which generates the non-overlapping clock which is required to operate the nMOS switches as shown in fig.14.

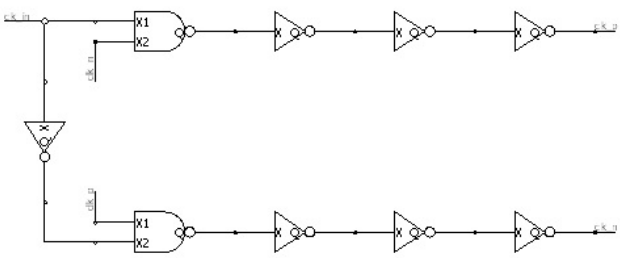

Fig. 13. Clock generator

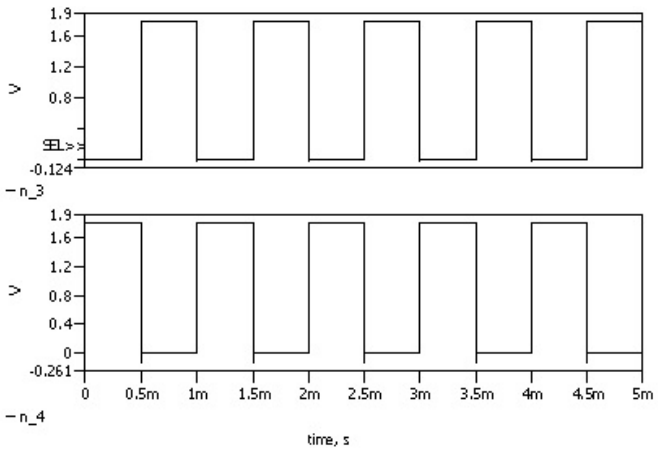

Fig. 14. Non-overlapping clock

C. Input impedance with parametric analysis

As mentioned in equation (1), the input impedance can be enhanced using decreasing the C_{in} or F_{chop}. In fig.15, the parametric analysis is shown which simply indicate that the input impedance is boosted by reducing the C_{in} however it additionally impacts on offset which is likewise a crucial parameter. Further, F_{chop} can't be decreased as it is dependent on the bandwidth of OTA. Therefore, a new method is integrated here.

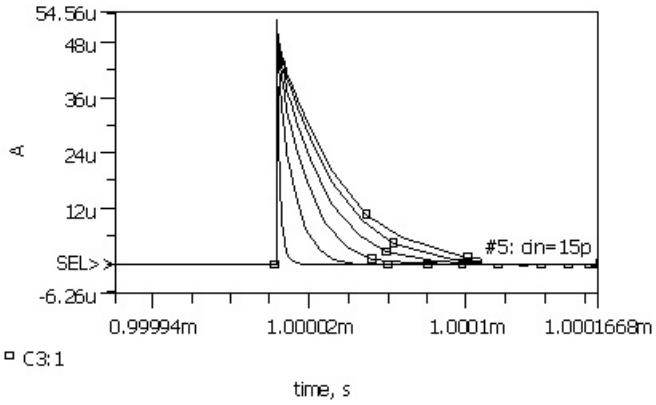

Fig. 15. DC input current for different C_{in}

In fig.16, the schematic to enhance the input impedance is shown wherein one forward auxiliary path is added in parallel to the input branch to lessen the total charge in capacitors C_{in}. So that the input DC current and subsequently the input impedance can be increased. Also, the input impedance is depending on the chopping frequency. So as according to the specification, the balancing among them could be very important as chopping frequency is likewise crucial to designing OTA to lessen 1/f noise.

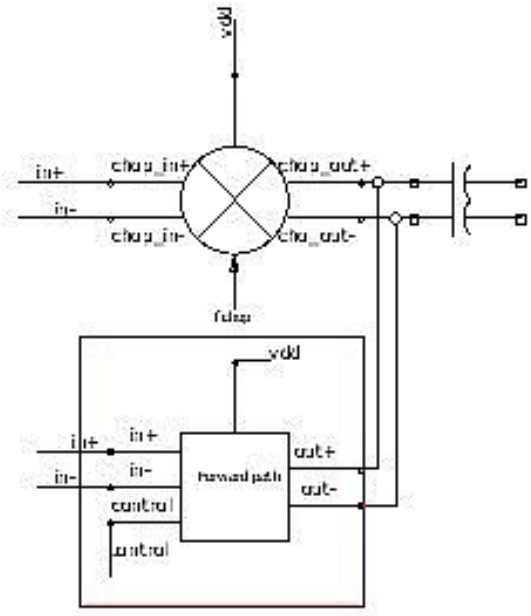

Fig. 16. Modification in input branch (with forward auxiliary path)

In the forward auxiliary path, the buffer with the gain of 40 dB and biasing current of 20nA is designed. It provides some power dissipation in total power consumption however this design can similarly be a concept like duty-cycled precharge of C_{in} utilizing managed buffer so that the extra power can be neglected in which in between precharge phase the forward path is unconnected by means of a control signal which is generated by the control block which is shown in fig.17.

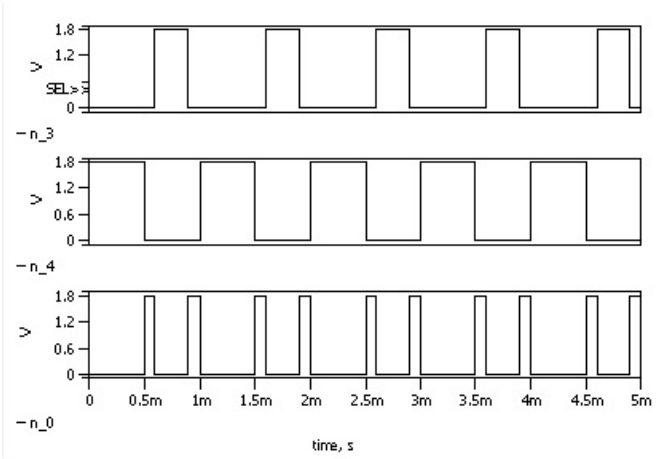

Fig. 17. Control signal for a buffer in the forward auxiliary path

In fig.18, the DC input current is shown with respect to time without using forward auxiliary path. In this, it has been observed that at the time of clock transition, some charges arise because of that the ensuring finite current increases which limit the input impedance which can be solved by the inclusion of forward auxiliary path as shown in fig.19.

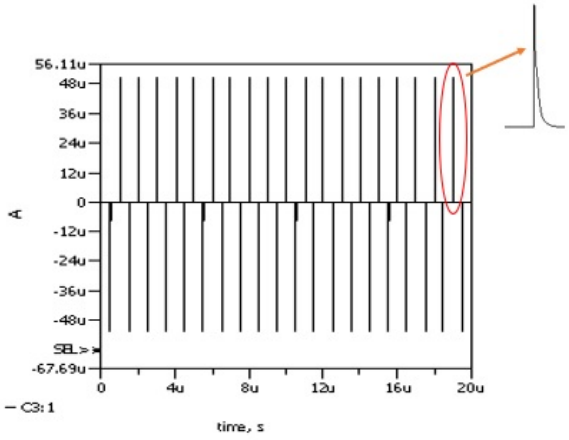

Fig. 18. Control signal for a buffer in the forward auxiliary path

D. Analysis of output ripple

In fig.20, the output branch of the OTA is shown. Here, the R-C network or DC blocking network is added at the output of an amplifier to reject the ripples.

In this design, the offset and the noise are exceeded through the chopper by once only so that the up-modulation of the offset and noise is passed off because of which the ripple is

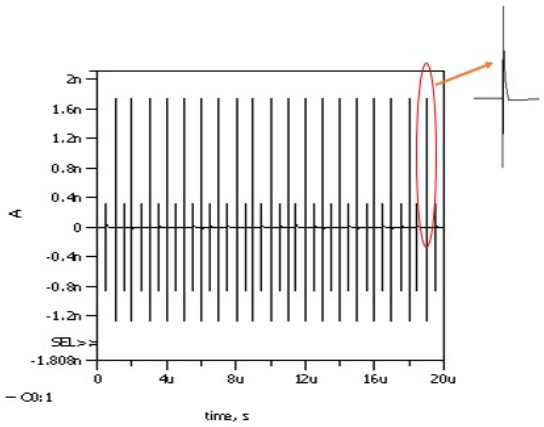

Fig. 19. Control signal for a buffer in the forward auxiliary path

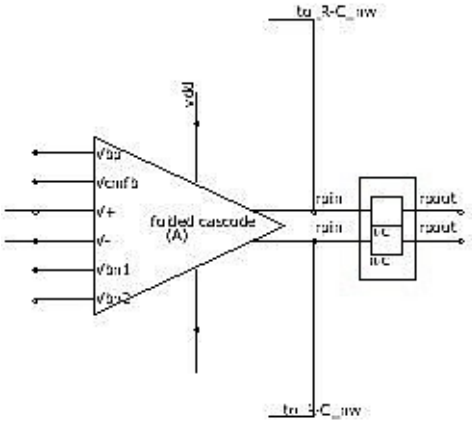

Fig. 20. Modification in output branch (with R-C dc block)

generated at the output. In fig.21, the simulation indicates the output waveform without the addition of R-C block. The R-C network has tuned this sort of manner that it is an open circuit for low frequency as its equivalent impedance is higher than the output impedance of the OTA and it is a short circuit at the chopping frequency so that desired signal can be passed and ripples due to up-modulated offset and noise are rejected. In fig.22, the output waveform after the inclusion of R-C block is shown.

E. Overall results

The periodic AC analysis of overall proposed design is shown in fig.23 which represents the gain of 100 or 40dB. In fig.24 and fig.25, the parametric periodic AC analysis is shown in which the response like high pass filter with the frequency band of 0.1KHz to 1KHz with different values of C_p and R_f respectively are analyzed.

The comparison analysis with different literature is shown in table II in which the parameters like power and noise is balanced and well suitable for such application and also input impedance is around 200MΩ which is fair enough for the biosignals recording and also the gain and CMRR has been optimized as per current state of art.

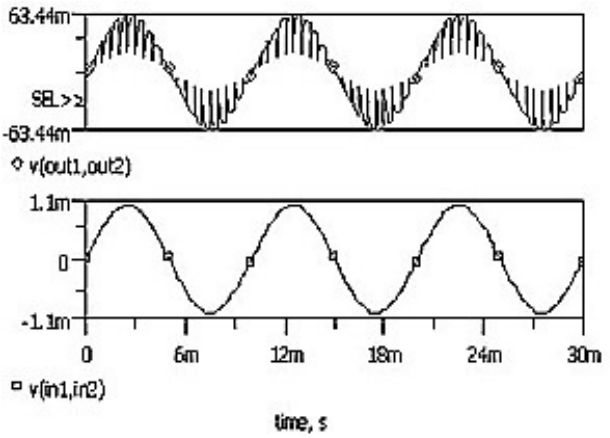

Fig. 21. Input current without R-C dc block

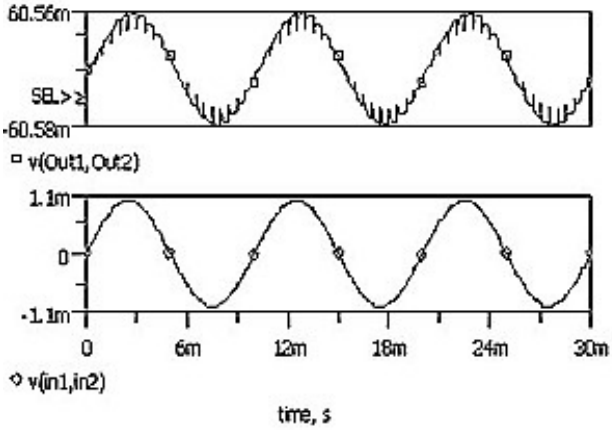

Fig. 22. Input current with R-C dc block

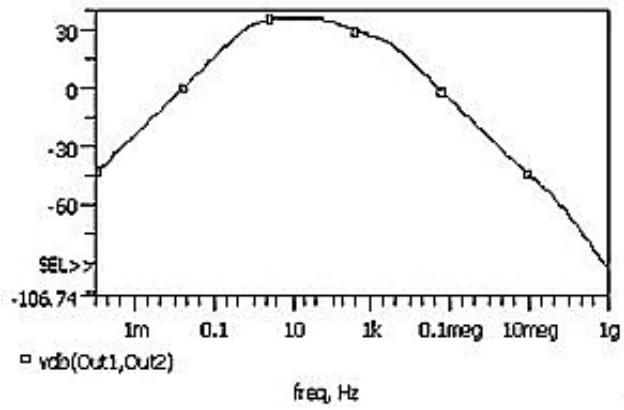

Fig. 23. Periodic AC analysis of biopotential amplifier

F. Layout

The floor plan and layout of the proposed design is shown in fig.26 and fig.27 respectively which is designed in the Magic layout tool. The total layout area of design is 279.8 by 177.1 μm^2.

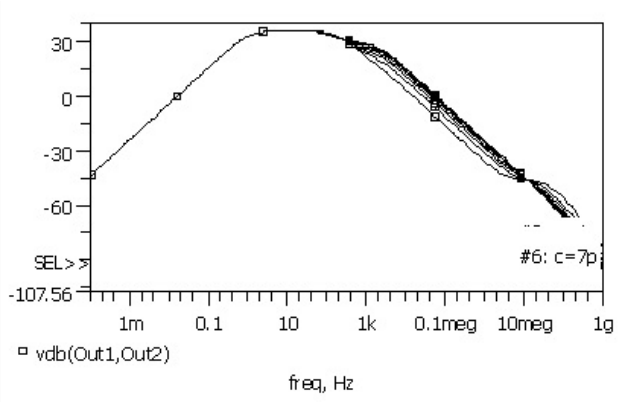

Fig. 24. AC analysis with different C_p

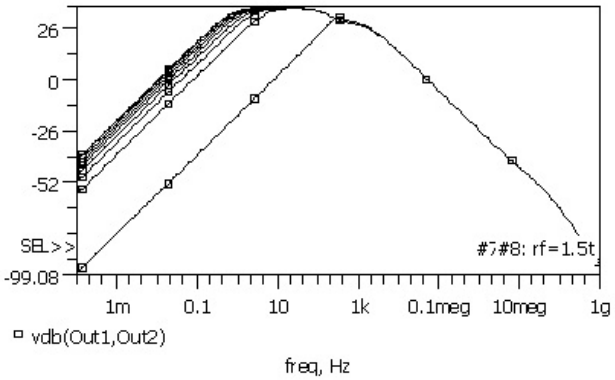

Fig. 25. AC analysis with different r_f

TABLE II
COMPARISON FROM SURVEY

Parameters	[2]	[10]	[17]	[18]	This work
Process(nm)	180	180	180	180	180
Supply(V)	1.8	1.25	1.8	2.7	1.8
Gain(dB)	34.7	-	30	40	40
Power(μ W)	4.2	2.12	75	-	5.5
Bandwidth(KHz)	0.1	10	1	2	1
CMRR(dB)	71.5	85	100	51	82
Noise(nV/$\sqrt{Hz}$)	250	45	75	3.76	42

IV. CONCLUSION

The proposed design of the biopotential amplifier is an improved architecture as compared to a conventional chopper amplifier. By including forward path and R-C network the input impedance is improved and output ripple in current is decreased. But the power consumption is increased due to additional buffer in the forward path but it is also reduced by controlled buffer using the control signal. To ensure lower power dissipation design uses only one OTA with removed low pass filter is used. Also, the band-pass response of an amplifier helps to reduce the offset and flicker (1/f) noise. The design is optimized for a DC gain of 40dB, with power dissipation of 5.5μW and noise of 42 nV/$\sqrt{Hz}$. Further, the input impedance is boosted (around 200MΩ) and offset is reduced around 10 μV.

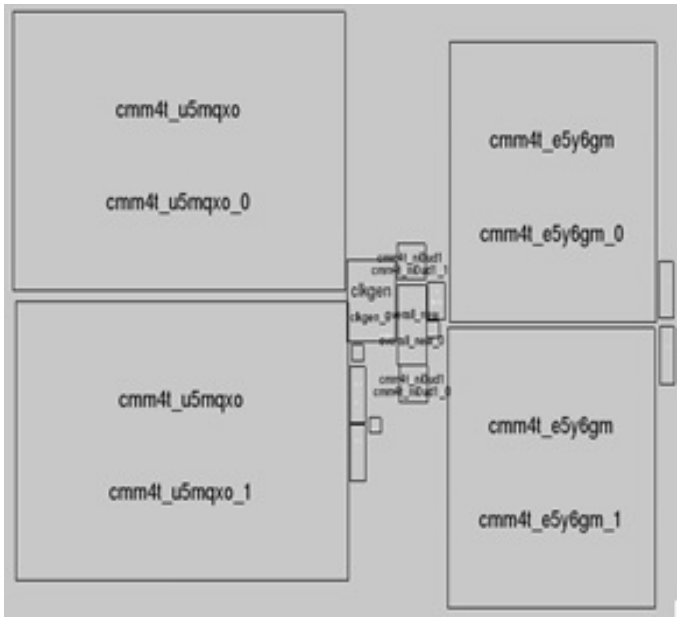

Fig. 26. Floorplan of an amplifier

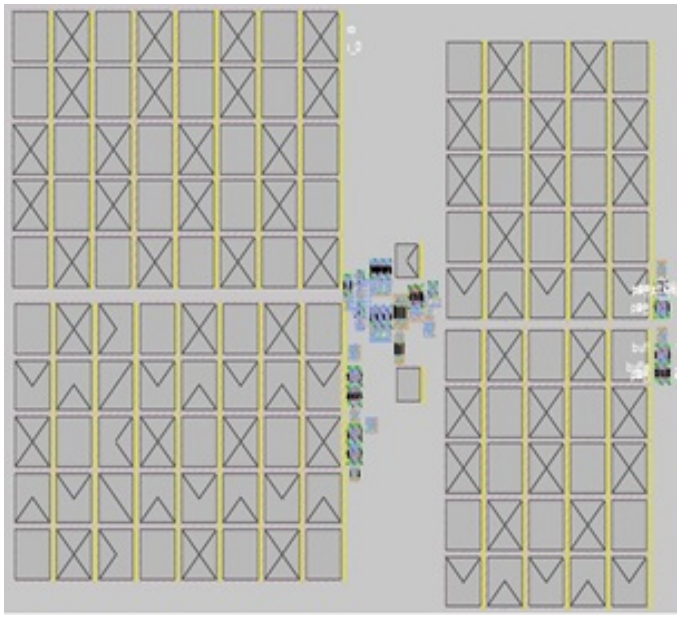

Fig. 27. Layout of an amplifier

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