

Double-gate MOSFET Model Implemented in Verilog-AMS Language for the Transient Simulation and the Configuration of Ultra Low-power Analog Circuits

Billel Smaani, Yacin Meraihi, Fares Nafa, Mohamed Salah Benlatreche, Hamza Akroum, and Saida Latreche

Abstract—This paper deals with the implementation of a DC and AC double-gate MOSFET compact model in the Verilog-AMS language for the transient simulation and the configuration of ultra low-power analog circuits. The Verilog-AMS description of the proposed model is inserted in SMASH circuit simulator for the transient simulation and the configuration of the Colpitts oscillator, the common-source amplifier, and the inverter. The proposed model has the advantages of being simple and compact. It was validated using TCAD simulation results of the same transistor realized with Silvaco Software.

Keywords—double-gate MOSFET, compact model, ultra low-power analog circuits

I. INTRODUCTION

THE multiple-gates (MG) field-effect transistors (FETs) are promising devices for the scaling of the bulk metal-oxide-semiconductor (MOS) FETs, especially for their immunity to short-channel effects (SCEs) [1-3]. The MG FETs are Silicon on insulator (SOI) MOSFET with several gates, such as the double-gate MOSFET, the triple-gate MOSFET, and the surrounding-gate MOSFET [4].

However, the double-gate (DG) MOSFET remain one of the best MG FETs architecture in terms of electrical performances and the simple process of fabrication. Therefore, the DG MOSFET is a very promising device for VLSI technology [5].

On the other hand, compact MGs FETs models coupled with circuit simulators are powerful tools for the design of analog and digital circuits with recent technology nodes [6], [7]. Moreover, the AC and DC behavior of the MGs FETs are well described with analytical compact models, which include small geometry effects, leakage current, and quantum confinement effects. In this case, the simplicity and the accuracy are significant parameters for the use of this type of models in the design and the simulation of analog and mixed circuits [8].

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In recent years, different compact models have been developed for MGs FET [9-11]. Just a few works have been carried out for the implementation of DG MOSFET compact models in the Verilog-A language [12-14], and most of the proposed works are dedicated to DC or AC models.

In this work, we have implemented a DC and AC double-gate MOSFET compact model in the Verilog-AMS language using SMASH circuit simulator for the transient simulation and the configuration of ultra low-power analog circuits, such as the Colpitts oscillator, the common-source amplifier, and the inverter. The proposed DC and AC model of the DG MOSFET is accurate, simple and compact.

Moreover, the Verilog-AMS language makes both Verilog-A and Verilog-HDL into the same MS-HDL language. Therefore, the Verilog-AMS offers a single language for the design of various circuits and systems with both analog and digital parts [15].

The paper is organized as follows. Section II presents the structure of the considered DG MOSFET transistor. Section III exposes the AC and DC model of the DG MOSFET transistor. Section IV gives the considered analog circuits: the Colpitts oscillator, the common-source amplifier, and the inverter. Section V presents the obtained results of the proposed model and circuits based on DG MOSFET. The last section concludes the paper and suggests some perspectives for future works.

II. STRUCTURE OF DG MOSFET TRANSISTOR

We consider an n-type symmetrical double-gate MOSFET transistor.

Indeed, Fig.1 illustrates the schematic view of the considered DG MOSFET transistor with the geometrical and technological parameters. Where L is the channel Silicon length, W ($=L$) is the channel silicon width, t_{ox} is the oxide thickness, and t_{si} is the Silicon thickness. V_{gs} and V_{ds} are the gate bias and the drain bias, respectively.

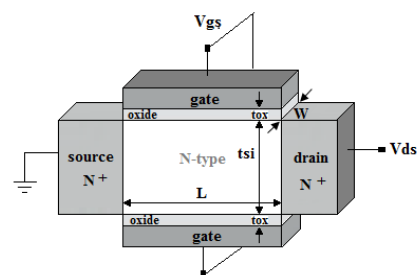


Fig. 1. Schematic diagram of the DG MOSFET transistor

III. MODEL DESCRIPTION

In the case of long channel n-type DG MOSFET and using the gradual channel approximation (GCA), the Poisson's equation can be written as [16], [17]:

$$\frac{d^2\Phi(y)}{dy^2} = \frac{q \cdot n_i}{\epsilon_{si}} \exp\left(\frac{\Phi(y) - V_{ch}}{\Phi_t}\right) \quad (1)$$

where $\Phi(y)$ is the electrostatic potential, q is the elementary charge, ϵ_{si} is the permittivity of silicon, n_i is the intrinsic carrier density, Φ_t is the thermal voltage, and V_{ch} is the quasi-Fermi potential in the channel.

Applying the Gauss law at the interface of the Silicon and the gate oxide, after a second integration of (1), we obtain the following expression [18], [19]:

$$V_{gs} - V_{ch} = -\frac{Q_m}{2.C_{ox}} + \Phi_t \cdot \ln\left(-\frac{Q_m^2}{8 \cdot \epsilon_{si} \cdot q \cdot n_i \cdot \Phi_t} - \frac{Q_m}{q \cdot n_i \cdot t_{si}}\right) \quad (2)$$

where Q_m is the mobile charge density per unit surface, C_{ox} is the oxide capacitance. It should be noticed that the mobile charge density can be computed iteratively from (2).

The drain-current model is obtained considering the drift-diffusion transport model through the integration of the mobile charge density in the channel (from Source to Drain) [1], [5]:

$$I_{ds} = -\mu \times \frac{W}{L} \int_0^{V_{ds}} Q_m \cdot dV_{ch} \quad (3)$$

where μ is low-field mobility.

Based on (3) and using (2), the expression of the drain-current for the DG MOSFET transistor can be presented as follows:

$$I_{ds} = \mu \cdot \Phi_t \times \frac{1}{2} \cdot \frac{W}{L} \times \left\{ Q_m \cdot \left(1 + \frac{Q_m}{2 \cdot \Phi_t \cdot C_{ox}} \right) + \frac{1}{2} C_{si} \cdot \Phi_t \cdot \ln \left(1 - \frac{Q_m}{8 \cdot \Phi_t \cdot C_{si}} \right) \right\}_{Q_{ms}}^{Q_{md}} \quad (4)$$

where C_{si} is the Silicon capacitance.

As result, Fig. 2 shows the variation of the modeled drain-current I_{ds} against the gate bias V_{gs} for two different values of the channel length ($L=1\mu\text{m}$ and 600nm).

As expected, we can note (from Fig. 2) that the current I_{ds} increase when the parameter L is decreased.

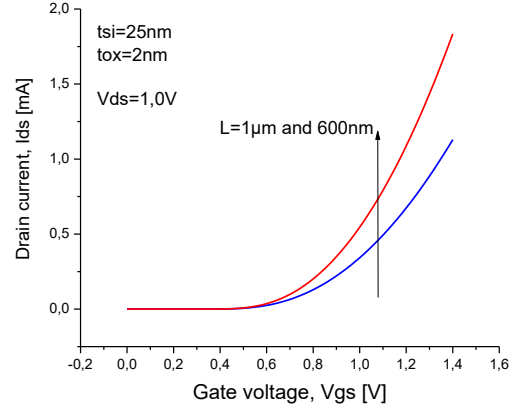


Fig. 2. Variation of the modeled drain-current I_{ds} versus the gate bias V_{gs} , for two various values of the parameter L

We define the capacitances of the DG MOSFET transistor as the derivative of the charges with respect to the terminals (gates, source, and drain), as follows [8], [20]:

$$C_{xy} = -\frac{\partial Q_x}{\partial V_y} \Big|_{x \neq y} = \frac{\partial Q_x}{\partial V_y} \Big|_{x=y} \quad (5)$$

where x, y stand for g, s and d (gate, source, and drain, respectively).

Using (5) and based on the EKV model for the MOSFET bulk [21], the gate to drain capacitance C_{dg} is given by:

$$C_{dg} = -1/15 C_{ox_T} \times \left\{ \left(4\chi_f^3 + 6\chi_r^3 + 28\chi_f^2\chi_r - 10\chi_f^2 - 15\chi_f\chi_r + 22\chi_f\chi_r^2 - 10\chi_r^2 \right) / \left(\chi_f + \chi_r \right)^3 \right\} \quad (6)$$

where C_{dg} is the gate to drain capacitance, $C_{ox_T} (= 2WLC_{ox})$

is the total oxide capacitance, $\chi_f = \sqrt{1/4 + q_{0s}^2 - q_{0s}}$ and

$\chi_r = \sqrt{1/4 + q_{0d}^2 - q_{0d}}$. With q_{0s} is the normalized charge in the source side and q_{0d} the normalized charge in the drain side.

Similarly, the gate to source capacitance C_{sg} is given by:

$$C_{sg} = 1/15 \cdot C_{ox_T} \times \left\{ \left(4\chi_r^3 + 6\chi_f^3 + 28\chi_r^2\chi_f - 10\chi_r^2 - 15\chi_f\chi_r + 22\chi_r\chi_f^2 - 10\chi_f^2 \right) / \left(\chi_f + \chi_r \right)^3 \right\} \quad (7)$$

As shown in Fig. 3, we can see the variation of the normalized gate-to-gate capacitance C_{gg} ($=C_{sg}-C_{dg}$), gate to source capacitance C_{sg} and gate to drain capacitance C_{dg} against the gate bias V_{gs} .

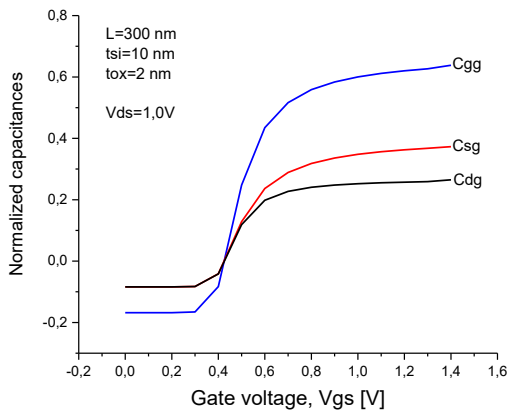


Fig. 3. Variation of the normalized main capacitances (C_{gg} , C_{sg} , and C_{dg}) versus the gate bias V_{gs} .

Additionally, the source to drain capacitance C_{ds} is given by:

$$C_{ds} = \frac{2}{15} C_{ox_T} \times \left\{ \left((2\chi_f - 1) + (\chi_f^2 + \chi_r^2 + 3\chi_f\chi_r) \right) / (\chi_f + \chi_r)^3 \right\} \quad (8)$$

Also, the explicit expression of the drain to source capacitance C_{sd} is given by:

$$C_{sd} = -\frac{2}{15} C_{ox_T} \times \left\{ \left((2\chi_r - 1) + (\chi_f^2 + \chi_r^2 + 3\chi_f\chi_r) \right) / (\chi_f + \chi_r)^3 \right\} \quad (9)$$

It is worth noticing that the capacitances C_{gs} , C_{dd} , C_{ss} , and C_{gd} are directly calculated using the other capacitances (6), (7) (8), and (9). With C_{gs} is the source to gate capacitance, C_{dd} is the drain to drain capacitance, C_{ss} is the source to source capacitance and C_{gd} is the drain to gate capacitance.

IV. CONSIDERED ANALOG CIRCUITS

Based on the DG MOSFET transistor, we have considered different types of low power analog circuits: the Colpitts oscillator, the common-source amplifier, and the inverter.

Fig.4, illustrates the circuit diagram of the DG MOSFET Colpitts oscillator [22-24].

To get a stable oscillation, the system in Fig.4 must satisfy the Barkhausen criteria:

$$\beta(w_0).G(w_0) = 1 \quad (10)$$

Where $G(w_0)$ is the gain of the amplifier (DG MOSFET) and $\beta(w_0)$ is the attenuation introduced by the tank (LC).

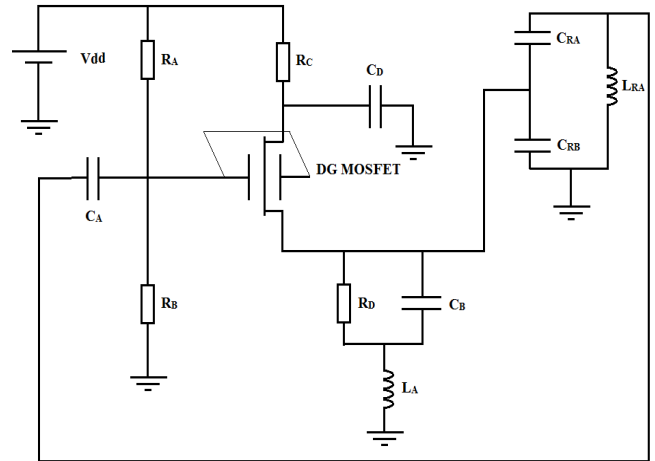


Fig. 4. Schematic view of the DG MOSFET Colpitts oscillator.

Then, the oscillation frequency is determined by the LC tank as:

$$w_0 = 1 / \sqrt{L.C_{eq}} \quad (11)$$

with $C_{eq} = C_{RA}.C_{RB} / (C_{RA} + C_{RB})$.

Table I indicates the electrical parameters of the DG MOSFET Colpitts oscillator. The values of the components were selected to assume an operating point in the linear region and also to get a stable oscillation.

Fig.5 and Fig.6 show the circuit diagram of the DG MOSFET common-source amplifier and the circuit diagram of the DG MOSFET inverter, respectively. In both cases, the active and passive electronic devices were selected for the good behavior of the considered circuits. Also, for the amplifier circuit, the electronic components were selected to have an operating point in the linear region and to assume an appreciable amplification.

Table II shows the electrical parameters of the DG MOSFET common-source amplifier.

TABLE I
PARAMETERS OF THE DG MOSFET COLPITTS OSCILLATOR

Parameters	Symbol	Value
Resistances (Ω)	R_A	75K
	R_B	120K
	R_C	50
	R_D	50
Capacitances (F)	C_A	5n
	C_B	10n
	C_D	10n
	C_{RA}	3p
	C_{RB}	2p
Inductances (H)	L_A	30n
	L_{RA}	1 μ

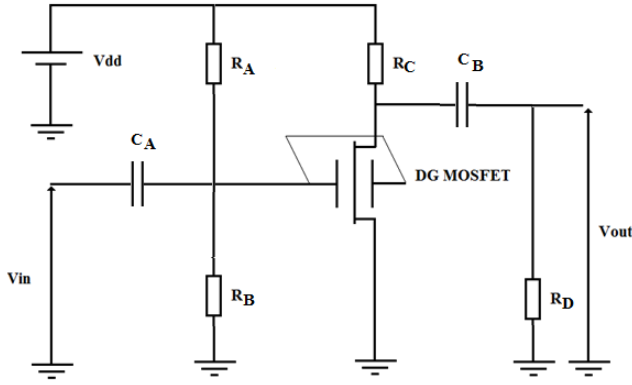


Fig. 5. Schematic view of the DG MOSFET common-source amplifier

TABLE II

PARAMETERS OF THE DG MOSFET COMMON-SOURCE AMPLIFIER

Parameters	Symbol	Value
Resistances (Ω)	R_A	100K
	R_B	100K
	R_C	250
	R_D	200
Capacitances (F)	L_A	10 μ
	L_{RA}	10 μ

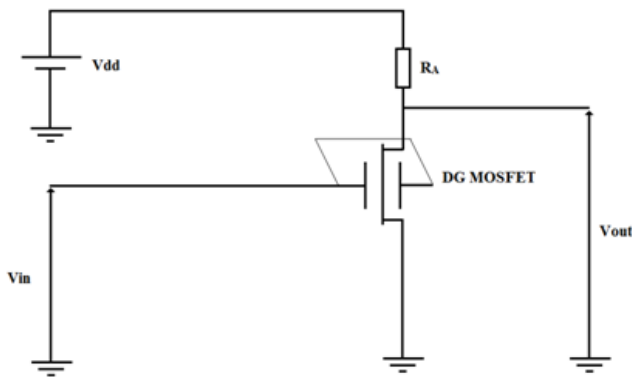


Fig. 6. Schematic view of the DG MOSFET inverter

V. RESULTS AND DISCUSSIONS

All of the considered analog circuits shown in Figs.4, 5, and 6 are based on the DG MOSFET transistor (Fig.1). The DC and AC behavior of this transistor are described using the analytical compact model detailed in section III. Then, the model is implemented in Verilog-AMS language using the SMASH circuit simulator [25].

Fig.7 presents the variation of the drain-current I_{ds} against the gate bias V_{gs} for different values of the drain bias V_{ds} (0.2, 0.5 and 1V). In this case, the results of the model in the Verilog-AMS are compared with the numerical simulation results of the DG MOSFET obtained with the Silvaco-TCAD [26]. We can note the good agreement in all operation regimes between both the TCAD simulation (dash) and the model implemented in Verilog-AMS language (line).

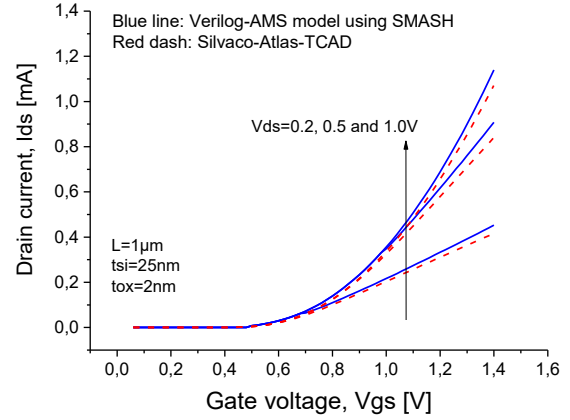
Fig. 7. Comparison of the $I_{ds}(V_{gs})$ characteristics using Verilog-AMS with Atlas-TCAD simulations, for various values of V_{ds} .

Fig.8 illustrates the computed gate-to-gate capacitance C_{gg} using the model in Verilog-AMS compared with the TCAD simulation results. As expected, the model using Verilog-AMS (line) shows a good agreement with the TCAD simulation results (dash).

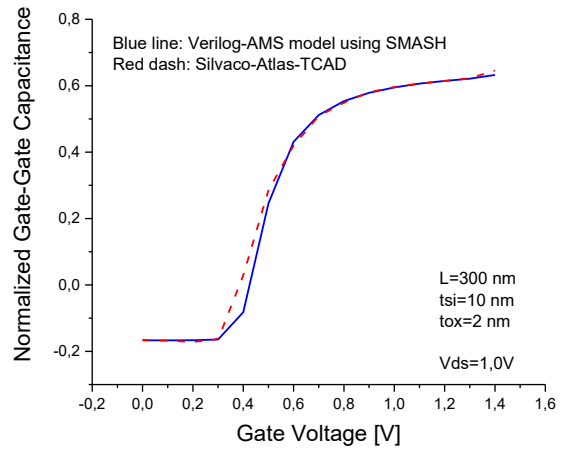
Fig. 8. Comparison of the $C_{gg}(V_{gs})$ characteristics using Verilog-AMS with Atlas-TCAD simulations

Fig.9 shows the variation of the output voltage for the DG MOSFET Colpitts oscillator obtained with the DG MOSFET model using Verilog-AMS and SMASH circuit simulator. The considered parameters of DG MOSFET are 25nm of the Silicon thickness, 1 μ m and 700nm of the channel length, and 2nm of the oxide thickness.

We can see in Fig.9 the stability of the generated oscillation and especially the dependence of the time delay with the reduction of the device channel length L . Therefore, we have found that reducing the device channel length L creates an important variation in the amount of the inversion charge and the current I_{ds} , which allows for a slower time delay. Moreover, reducing the DG MOSFET parameters reduces the oscillator circuit size and makes the DG MOSFET an excellent candidate for RF (Radio Frequency) oscillator circuits. Also, the frequency oscillation is almost equal to 0.17 GHz.

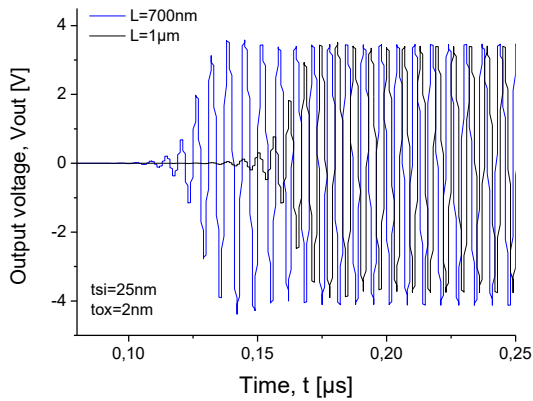


Fig. 9. The output voltage of the DG MOSFET Colpitts oscillator obtained using Verilog-AMS and SMASH circuit simulator, for various values of L

Fig.10 shows the result of the transient simulation for the DG MOSFET common-source amplifier, obtained using the DG MOSFET model implemented in Verilog-AMS with SMASH. The efficacy of the amplifier can be observed through the input signal (blue line) and the output signal (black line).

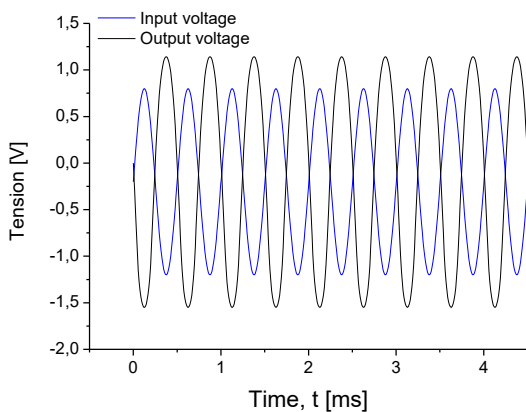


Fig. 10. Transient response of the DG MOSFET common-source amplifier obtained using Verilog-AMS and SMASH circuit simulator, with $L=1\mu\text{m}$, $t_{si}=25\text{nm}$, and $t_{ox}=2\text{nm}$

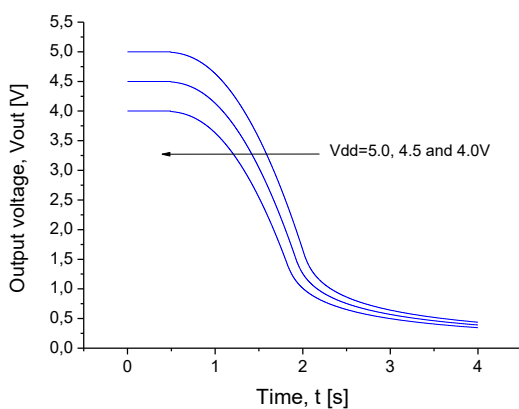


Fig. 11. Transient response of the DG MOSFET inverter obtained using Verilog-AMS and SMASH circuit simulator, for various values of V_{dd}

Fig.11 shows the result of the transient simulation for the DG MOSFET inverter, obtained using the DG MOSFET model implemented in Verilog-AMS with SMASH. For different values of the voltage V_{dd} (4, 4.5, and 5V) the inverter has a good transient answer and excellent behavior.

CONCLUSION

We have implemented a DC and AC DG MOSFET model in Verilog-AMS language targeting the transient simulation and the configuration of ultra low-power analog circuits. A physics-based compact model was established to describe DC and AC electrical behavior of the DG MOSFET and low-power analog circuits using Verilog-AMS and SMASH circuit simulators. A good agreement was observed between the results of the compact model using Verilog-AMS and TCAD simulation results. We have considered different types of analog circuits based on the DG MOSFET model using Verilog-AMS: the Colpitts oscillator, the common-source amplifier, and the inverter. We have found in the case of the Colpitts oscillator that the dependence of the time delay with the device channel length is very important. As expected, a smaller delay is obtained with the reduction of the device parameters, especially the channel length. Also, the simulation and the configuration of the common-source amplifier and inverter prove the efficacy of the Verilog-AMS script for the model. In addition, the proposed DG MOSFET model using Verilog-AMS language presents excellent usefulness for the simulation, configuration, and design of various types of ultra low-power analog circuits.

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