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Experiment on nearest level modulation algorithm for FPGA based Modular Multilevel Converters

Van Son Nguyen, Cuong Tran Hung, Pham Viet Phuong, Dung Hoang Anh, Giang Nguyen Hoai, and Nghia Hoang Trong

***Abstract*—Modular Multilevel Converter (MMC) has been applied to medium and high - voltage power systems recently because it has many advantages over other multilevel converters. This paper will present the algorithms of Nearest Level Modulation (NLM) and capacitor voltage balancing to greatly reduce the switching frequency as well as producing an output voltage at the AC side with very low harmonic distortion. The experimental system for the MMC converter requires a large amount of I/O signals ports. However, Digital Signal Processor (DSP) only provides up to 24 I/O signals ports while the experimental system of the MMC converter needs more than that. In this paper, the experimental system used FPGA to embed the proposed methods and applied to an MMC with 12 Sub-Modules (SM) to generate a 13-level AC voltage waveform. In this case, FPGA is the most suitable choice to develop the control circuit for the experimental system of MMC. The effectiveness of the proposed algorithm was verified by simulations and tested using a laboratory – scale prototype.**

***Keywords*—Experimental for MMC; FPGA for MMC; Nearest Level Modulation Modular Multilevel Converter; Sub-Modules**

I. Introduction

In recent years, research in high-power and high-voltage conversion systems has focused on multilevel converters [1] - [2]. Multilevel converters have many advantages over conventional two-level converters in term of application in medium and high voltage areas [3] – [5], [8]. Some of the advantages that can be mentioned as follows: (i) Low switching frequency operation mode can be achieved to reduce the voltage stress on the switching devices; (ii) The voltage level can be increased at a low switching frequency which is good in helping the converter to operate more stable. The MMC converter is a new multilevel converter based on modular structure with many promising advantages for high voltage applications. MMC can be expanded to achieved a waveform at any number of volatge levels with low harmonics distortion as well as the capability of operating at any power ratings. The most attractive advantage of MMC is that it does not require individual dc sourse for each sub-module but only a single DC bus voltage [6], [9]. However, the operation of MMC has some disadvantages such as voltage imbalance of capacitors in each phase [3] and the experimental process requires many I/O signal ports to connect to the control system [7], [10]. Among the modulation methods for miltilevel converters, the NLM has played an important role as the most suitable modulation method for MMC. It can calculate accurately the number of SMs that need to be "inserted" or "bypassed" to generate the desired output voltage level with reduced switching frequency [8]. This method has a simple implementation and has addressed the disadvantages of PWM and SVM modulation methods [9]. Several experimental studies of MMC have been presented as in the references [7] and [10]. However, the NLM modulation method has not been experimentally applied to the 12-SMs MMC for generating a 13-levels AC voltage waveform. The experimental system of the MMC with the capability of implementing of NLM method and balancing the capacitor voltage requires a large number of I/O ports, which creates significant difficulties in terms of complicated as well as the limitation in I/O signal ports of the DSP. Current DSPs can only provide 24 I/O signal ports which are insufficient to meet the requirements for 42 I/O signal ports in 13-levels AC voltage MMC converters. FPGA have been used instead of DSP to implement the NLM modulation algorithm for MMC because of its advantages such as the flexibility in solving complex program and the connectivity issues. This has reduced the cost and time of implementing the system, and made it more compact, allowing for the design of highly complex digital control systems [7]. Due to their flexibility and large number of I/O ports, FPGA can achieve high configurability [10], making it highly suitable for implementing NLM modulation techniques and high-precision capacitor voltage balancing algorithms for MMC. To test the system, first the values of current and voltage must be measured to send to the FPGA through the I/O ports. The modulation and control algorithms are implemented based on the Verilog programming language and generate real-time control signals. The dynamic responses of the MMC system under various steady-states are demonstrated by experimental results in real

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system. The results obtained from the experimental system and simulation are analyzed and compared to demonstrate the accuracy of the proposed algorithm. The structure of this article is as follows: The structure and operating principle of MMC are presented in summary in Section II. In Section III, NLM modulation method and capacitor voltage balancing algorithm are introduced. In Section IV, simulation and experimental results of the MMC system validate the proposed method.

II. Operation Principle of the MMC

Figure 1a illustrates the structure diagram of a three phases MMC. Each phase consists of two valve branches called upper and lower branches. Each branch consists of N identical SMs, which are connected in series with each other and in series with the inductor. Each SM consists of two IGBTs with anti-parallel diodes and a capacitor. The converter is supplied by a single DC source. The desired output voltage level is determined by the number of SMs connected in series in each phase. On each branch there is a inductor Lo. which limits the transient currents that may arise and current circulation between phases [4]. The operating principle of the MMC is based on the “insert” or “bypass” each SM according to a specific rule to create the voltage waveform of the MMC. In each modulation cycle, there will be an SM from the upper branch SM “insert” and a SM from the lower branch “bypass”, or vice versa. Therefore, only N SMs are included in a each modulation cycle. This process will generate an AC voltage at the output in which each voltage level has a value of VDC/N. This voltage value equals to that of the capacitor of each SM. As the number of SMs in each branch increases, the number levels of output voltage of the MMC will increase correspondingly. The output voltage levels of the MMC are limited to ±VDC/2 for AC output voltage. Figure 2 shows the ON and OFF status or also called the "insert" and "bypass" status of the SM. The positive-current case is shown as Figure 2a and the negative-current case is shown as Figure 2b.

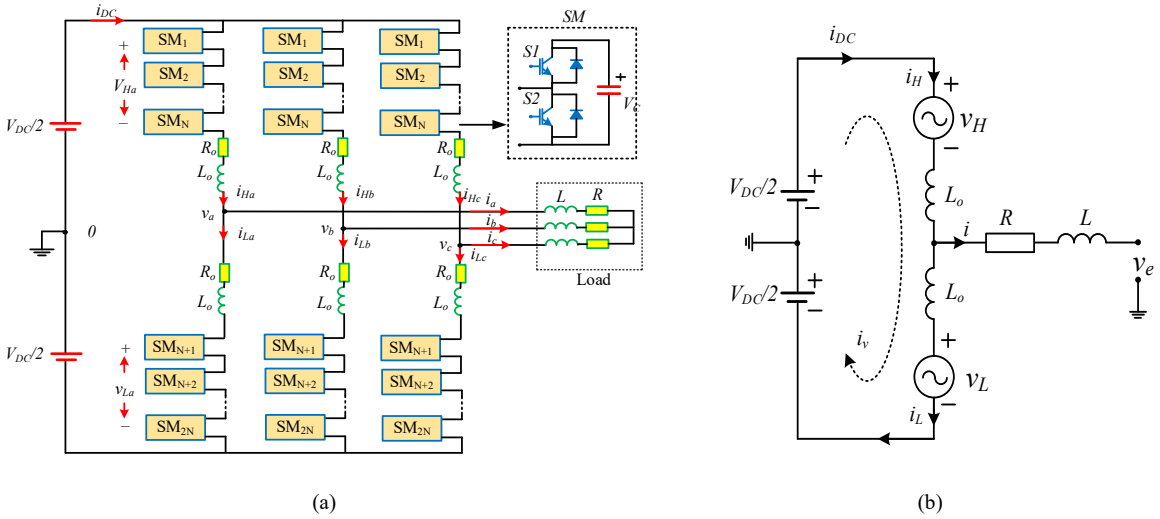


Fig. 1. (a) Structure of MMC, (b) principle diagram of MMC connected to a typical load

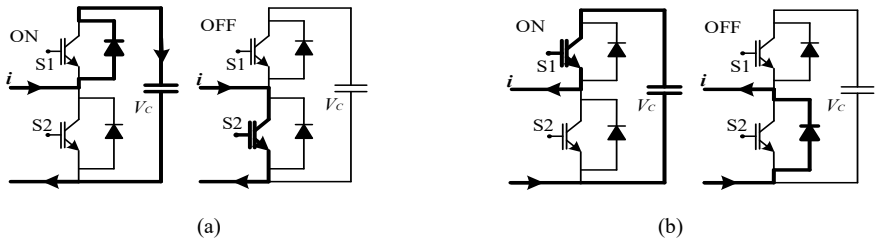


Fig. 2. State ON and OFF of the SMs when: a) positive current; b) negative current

When the output voltage of the SM equals to the capacitor voltage, the SM is "inserted", and when the output voltage of the SM is zero, the capacitor is "bypassed". Figure 1b shows the equivalent circuit for one phase of MMC. Where iDC and VDC are the DC current and voltage of MMC, VH and VL are the sum of the SM voltage in the upper and lower branches of each phase, iH and iL are the current in the upper and lower branches of each phase, ve and i are respectively the voltage and current at the AC side of MMC. Equation (1) represents the relationship between the AC current and the current in the upper and lower branches of MMC.

$$i = i_H - i_L \tag{1}$$

Due to the unique configuration, in each phase of the converter, there exists a circulating current iv which flows through the upper and lower branches. The circulating current is determined by Kirchhoff's law and is defined by Equation (2).

$$i_v = \frac{i_H + i_L}{2} \quad (2)$$

If bypass the voltage falls on the resistor and inductor on the AC side of the converter, the alternating voltage ve can be determined as:

$$v_e = \frac{1}{2}(v_L - v_H) \quad (3)$$

The component voltage vH and vL in equations (3) are calculated as:

$$\begin{cases} v_L = m_L V_{CL}^{\Sigma} \\ v_H = m_H V_{CH}^{\Sigma} \end{cases} \quad (4)$$

Where: V_{CL}^{Σ} and V_{CH}^{Σ} are the total inserted voltages of the upper and lower branches, the number of SMs inserted in the upper and lower branches are represented by the coefficients mL and mH and have values ranging from 0 to 1. When mL or mH equals 1, all SMs in the upper or lower branch are inserted.

III. APPLICATION OF NLM AND CAPACITOR VOLTAGE BALANCING ALGORITHM FOR MMC

The improved NLM method is used to increase the output voltage level of the MMC up to 2N+1. This method can be easily implemented with a low swiching frequency and can address the disadvantages of PWM and SVM modulation methods, as well as reduce the total harmonic distortion of the MMC [8]. The operating principle of the improved NLM method for the MMC with 10-SMs in each branch is described as in Figure 3.

$$\begin{cases} N_L = round_{0,25}\left\{\frac{V_{DC}}{2V_C}\left[1 - m\cos(\omega t)\right]\right\} \\ N_H = round_{0,25}\left\{\frac{V_{DC}}{2V_C}\left[1 + m\cos(\omega t)\right]\right\} \end{cases} \quad (5)$$

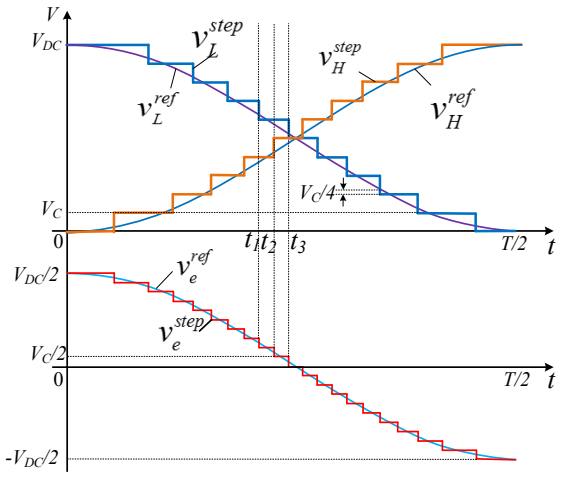


Fig. 3. Principle of modified NLM method

In this method, the step height of the output voltage is $0.25V_c$, leading to an increase in the output voltage level and making the output voltage waveform more sinusoidal. To achieve this, the algorithm used a round function as in equation (5). The implementation process of the NLM method is analyzed in two times intervals: [t_1, t_2] and [t_2, t_3], as shown in Figure 3. In the first times interval [t_1, t_2], the reference values of the voltage branch and the AC output voltage at t_1 will be set as follows:

$$\begin{cases} v_L^{ref} = (M + 0,25)V_C \\ v_H^{ref} = \left[(N - M - 1) + 0,75\right]V_C \\ v_e^{ref} = (M - 0,5N + 0,25)V_C \end{cases} \quad (6)$$

According to the round function, the step waveforms of the arm voltage and AC voltage in the first case are expressed as in equation (7):

$$\begin{cases} v_L^{step} = MV_C \\ v_H^{step} = (N - M)V_C \\ v_e^{step} = (M - 0,5N)V_C \end{cases} \quad (7)$$

The second case is from t2 to t3. The reference voltage for each branch and the AC voltage at t2 are determined by equation (8) as follows:

$$\begin{cases} v_L^{ref} = \left[(M - 1) + 0,75\right]V_C \\ v_H^{ref} = \left[(N - M) + 0,25\right]V_C \\ v_e^{ref} = (M - 0,5N - 0,25)V_C \end{cases} \quad (8)$$

The step waveform of the arm voltage and AC voltage in this case are expressed as in equation (9):

$$\begin{cases} v_L^{step} = MV_C \\ v_H^{step} = (N - M + 1)V_C \\ v_e^{step} = (M - 0,5N - 0,5)V_C \end{cases} \quad (9)$$

Comparing equations (7) and (9), it can be seen that the height of the step in v_e^{step} is 0.5V while comparing equations (6) and (7) or (8) and (9), the maximum error is 0.25VC.

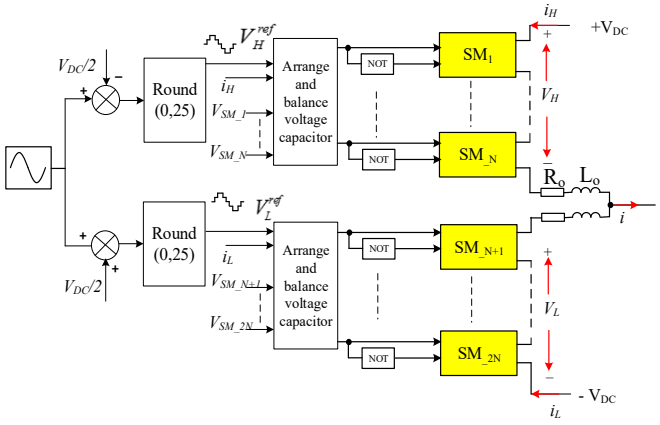


Fig. 4. Structure 1-phase of MMC uses NLM method

Algorithm for capacitor voltage balancing for the SMs of the MMC is shown in Fig. 4. Some methods related to capacitor voltage balancing have been studied in the references [12] and [13]. Capacitor voltage balancing is an important issue in the operation of MMC. The reason is that the capacitors of the SMs have different values during their operation. As the number of SMs on each arm is large, voltage balancing based on the voltages arrangement of the capacitors to select which SMs to be "inserted" is the method that is more suitable than other methods.

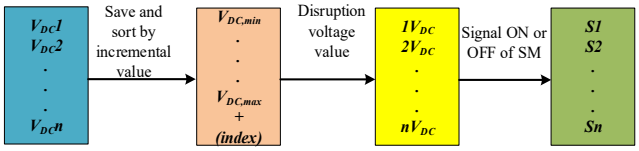


Fig. 5. Diagram principle of capacitor voltages arrangement in balance algorithm

The capacitor charging process is carried out as follows upon request: after the NLM algorithm determines the number of SMs need to be "inserted" to generate the desired output voltage level at one time, the voltage balancing algorithm will arrange the capacitor voltage of all SMs based on the direction of the current to select the SMs, those will be "inserted" or will be "bypassed". This method has the advantage of minimizing the difference between the voltage across the capacitors of the SMs and the reference voltage [13].

$$\begin{cases} V_{DCi} > V_{avg} + \Delta V & Charge \\ V_{DCi} < V_{avg} - \Delta V & Discharge \end{cases} \quad (10)$$

Where: ΔV is the threshold value of the capacitor voltage determined based on the voltage balancing target on the capacitor. The process of arranging the capacitor voltage values in the voltage balancing algorithm is shown in Figure 5.

IV. Modeling of Control Circuit and Results

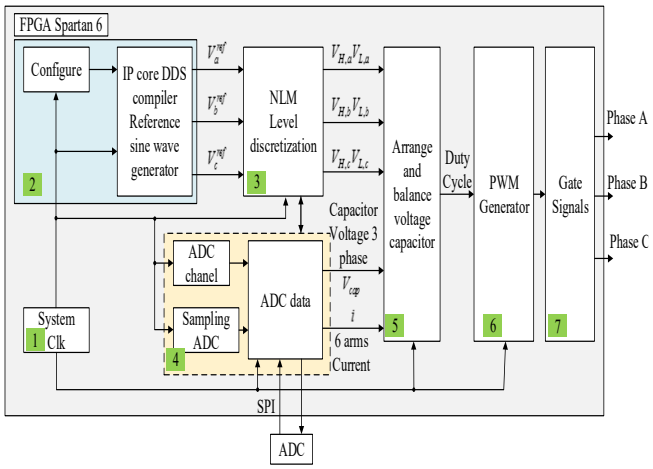


Fig 6. Block diagram of NLM modulation algorithm

A. Application of FPGA to control the MMC

Figure 6 shows the block diagram of the NLM modulation algorithm when implemented in FPGA for experimental purpose. The functions of each specific blocks are as follows:

1) System Clock: This is a pulse generator block with a pulse frequency of 50MHz in FPGA device.

2) Reference sine wave generator: This block generates three sine waves with a frequency of 50Hz and a phase difference of 120 degrees. These three waves are then fed into the IP core DDS compiler in a Look-up-table form.

IP core DDS compiler Reference sine wave generator: Phase with 32 bits, output with 8 bits. Code to set the value:

" begin
a_pinc_in<=32'd4295; // f = 50Hz
a_poff_in<=32'd0; //phase a
b_pinc_in<=32'd4295; // f = 50Hz
b_poff_in<=32'd1431655765; //phase b
c_pinc_in<=32'd4295; // f = 50Hz
c_poff_in<=32'd2863311531; //phase c
end"

3) NLM Level discretization: This block will automatically calculate and generate the necessary voltage level for each valve branch.

4) ADC communication block: This block will sample ADC signal with a sampling frequency of 100kHz; The ADC channel consists of 6 MCP3208 ADCs with 8 output channels, communicating via SPI, It has 6 channels for measuring current and 36 channels for measuring voltage.; ADC data: Establish SPI communication with ADC and save the measured ADC values.

5) Arrange and balance voltage capacitor: This block will calculate the pulse generation time for each IGBT valve.

6) PWM Generator: This block will generate time intervals for turn on and turn off IGBT valves.

7) Gate Signals: this block defines the signal ports for transmitting pulses.

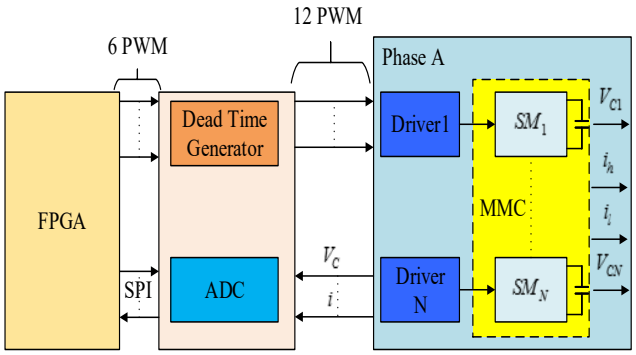


Fig. 7. The general structure of the system for phase A

TABLE I
FPGA Resources

Used FPGA Resources		
Number of Slice Register (Flip-Flops)	51	%
Number of Slice LUTs	18	%
Number of MUXCYs used	88	0%
Number of occupied Slices	76	2%
Number of bonded IOBs	8	0%

Figure 7 illustrates the general structure of the system for phase A, where each SM requires 2 PWM signals from its output, which are inverted signals performed by the Dead Time circuit. Table 1 presents the FPGA resources used to implement each modulation technique. Control programs are performed on Xilinx ISE Design Suite AX309 and blocks in Figure. 6 are created in Verilog language, then Tool Create Schematic in Design Utilities is used to create the Schematic file.

Because the PWM signals from the FPGA are at 3.3V which is not sufficient to drive the IGBTs. Therefore, the system uses the HCPL 316j driver in combination with a Dead Time circuit to increase the voltage level to 15V. The specifics of the work process are described as follows: the Synthesized-XST Tool is

used to synthesize the schematic model of the switch control circuit. The input/output ports are assigned according to the available pin configuration of the Xilinx Spartan-6 FPGA development board using the PlanAhead tool. Once the PlanAhead is closed by selecting the Exit tab, a ucf file is added to the project, which contains the constraints. The design Summary viewer reports timing constraints, pin out report, errors & warnings and other information. It is essential to check the pinout report carefully especially whether or not all signals have been assigned to the correct FPGA pins. After verification, a configuration bitstream is created for the model. The process tab Generate Programming File can be used to generate a bit file to program the FPGA. The FPGA board is connected with the PC through a standard USB cable on the USB based download/debug port of the test board. The FPGA is programmed using the IMPACT tool under the Configure Target Device process.

Fig. 8. Experimental system of MMC: 1. Driver; 2. V_{DC}; 3. Load; 4. Measure circuit; 5. FPGA; 6. ADC

Fig. 8 shows the structure diagram and experimental system of MMC. The processing signals are executed by Xilinx ISE Design Suite AX309 kit as this device has a sufficient number of I/O pins with the capability of flexible and fast signal processing speed. The FPGA will implement the NLM modulation algorithm and send control signals to close or open IGBT valves of the MMC. The algorithm implementation of the FPGA consists of following steps: (i) Generate three reference sine wave signals having phase difference of 120º; (ii) Implement the round function of voltage steps based on the improved NLM modulation algorithm; (iii) Implement the capacitor voltage balancing algorithm for the SMs; (iv) Send control pulses to IGBT valves of each SM. In this paper, we will show the simulation and experimental results of the MMC with 6 SMs per arm or 12 SMs in each phase with parameters shown in Table 2.

TABLE II
SPECIFICATIONS ON 3 PHASE OF MMC

Symbol	Value	Symbol	Value
V_{DC}	400V	L	70 mH
C	25 mF	SM	12
R_o	0,01 Ω	F	50 Hz
L_o	mH		

B. Simulation and experimental results

The pulse generator diagram from the FPGA driver circuit for each SM of phase A is illustrated in Figure 9. The gate pulses for other SMs will have similar shapes. Figure 9 shows that the pulse from FPGA and Driver has no latency and has standard square pulse form. This proves that the system's circuit elements are stable and ready to implement the proposed modulation algorithms.

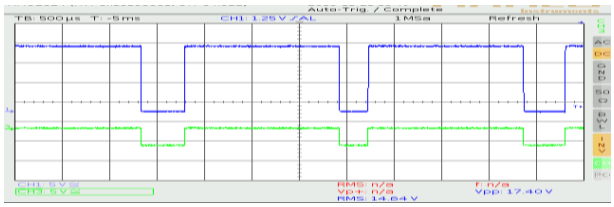
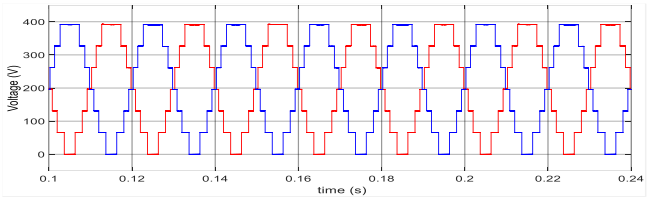
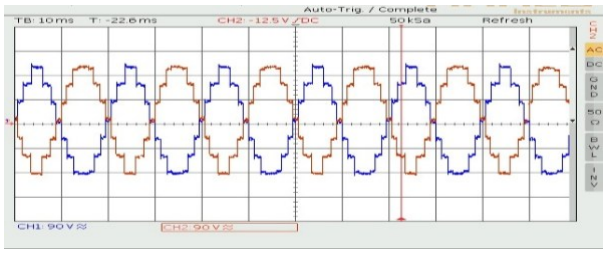


Fig. 9. Sample pulse output of FPGA and Drive provided for IGBT

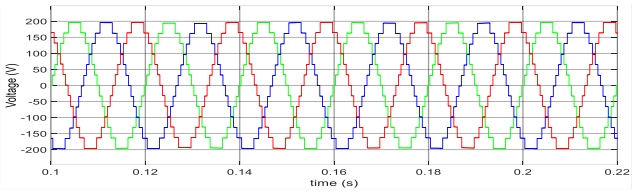


(a)

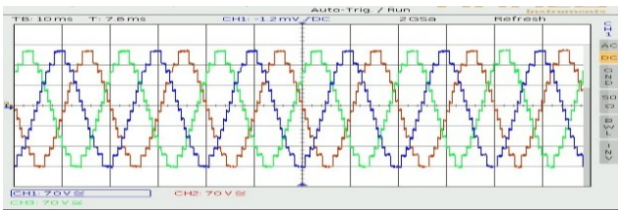


(b)

Fig. 10. The voltage of the upper and lower arms of the MMC, (a) Simulation result; (b) Experimental result



(a)



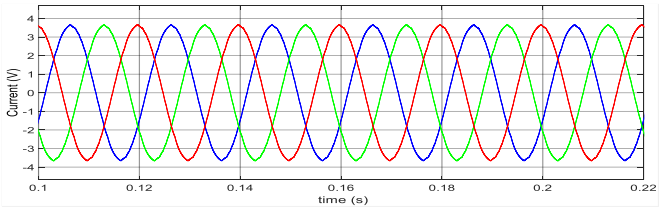
(b)

Fig. 11. Phase voltage at the AC side of the MMC converter, (a) Simulation result; (b) Experimental result

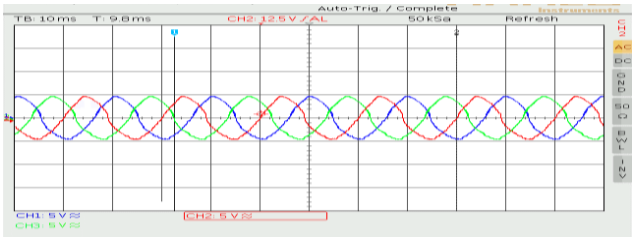
The voltage waveforms of the upper and lower arms on a phase of the MMC converter in simulation and experimental are depicted in Figure 10. These voltages have 7 voltage levels due to the execution of the round function in (5) to calculate the number of SMs needed to be "inserted".

The simulation results of the phase voltages at the AC side of the MMC are shown in Figure 11a while the experimental results of that are shown in Figure 11b. The results show that the voltage waveforms have 13-levels which are true as the theoretical description.

The simulation results of the phase current at the AC side of the MMC are shown in Figure 12a while the experimental results are shown in Figure 12b. Both waveforms show that the current are sinusoidal as expected.



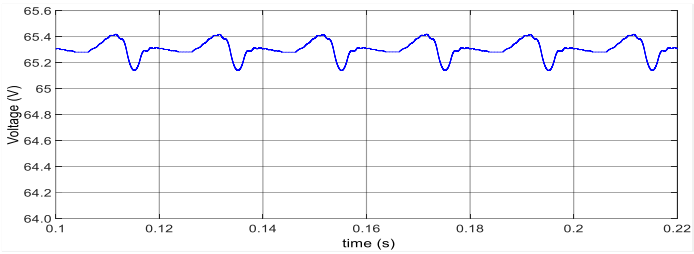
(a)



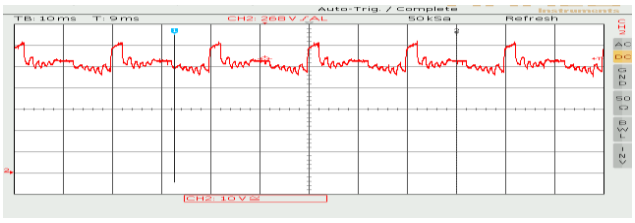
(b)

Fig. 12. Phase current at the AC side of the MMC converter, (a) Simulation result; (b) Experimental result

The simulation and experimental results of the capacitor voltage of one SM in phase A are shown in Figures 13a and 13b. Both waveforms show the success of the balancing mechanism based on a sub-module selection process. The results have met the goals set out by the algorithm proposed in this paper and met the goals of MMC.



(a)



(b)

Fig. 13. Capacitor voltage of SM1 in phase A, (a) Simulation results; (b) Experimental

CONCLUSION

The authors of this paper have succeeded in applying the Nearest Level Modulation and capacitor voltage balancing algorithms to a MMC converter for the purpose of reducing the switching frequency as well as the harmonic components of the voltage at the AC side. The experiment system in this paper used the FPGA to implement the modulation algorithm and control technique for the MMC. Both simulation and experiment results were agreed well to each other and met the goals set out by the authors of this paper.

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