

# DTMOS Based Bandgap Reference Design in CMOS 28nm Process

Filip Księżyc, and Piotr Kmon

**Abstract**—This paper describes design and simulation results of the bandgap reference source in CMOS 28nm technology. Proposed bandgap reference utilizes DTMOS transistors for providing currents of negative and positive temperature coefficients and is equipped with various techniques for process variation minimization such as common centroid element design and user controlled trimming resistors. This circuit achieves temperature coefficient equal to  $-18.87 \text{ ppm}/^\circ\text{C}$  with temperature ranging from  $-20^\circ\text{C}$  to  $100^\circ\text{C}$  at 1V power supply, occupies  $0.38 \text{ mm}^2$  of silicon area, and consumes  $3.66 \text{ }\mu\text{W}$  of power.

**Keywords**—bandgap reference; DTMOS; CMOS 28nm

## I. INTRODUCTION

BANDgap references as a concept are crucial blocks responsible for providing stable reference (either current or voltage) for many widely used analog and digital electronic devices such as filters, memory blocks, oscillators and of course A/D converters [1] – [4]. Photonic detectors [5] – [7] also need stable reference immune to temperature, supply voltage, and process variation as reference is there crucial for precise correction of main integrated circuit (IC) parameters such as photons' energy threshold, setting proper circuit biasing point or improving the ICs immunity in harsh environment conditions. Any variation of reference may influence the recorded data especially when the purpose of circuit is its high precision.

Based on that fact we decided to design a reference circuit that will be compatible with modern CMOS processes and its implementation example is presented in this paper. Presented bandgap reference circuit uses DTMOS (Dynamic Threshold Metal Oxide Semiconductor) transistors as a source of positive and negative temperature current coefficients and achieves  $-18.87 \text{ ppm}/^\circ\text{C}$  temperature coefficient of output reference current.

This paper presents brief introduction to idea of bandgap reference circuits based on DTMOS devices, design of bandgap reference circuit with layout floorplan and results of simulations performed on the extracted model.

## II. BANDGAP REFERENCE CIRCUIT

Idea of providing reference voltage, that is independent of temperature variation is based on four major blocks, that are shown in Fig.1.

Filip Księżyc (email: fksiezyc@agh.edu.pl) and Piotr Kmon (email: kmon@agh.edu.pl) are with Department of Measurement and Electronics, Faculty of Electrical Engineering, Automatics, Computer Science and Biomedical Engineering, AGH University of Krakow.

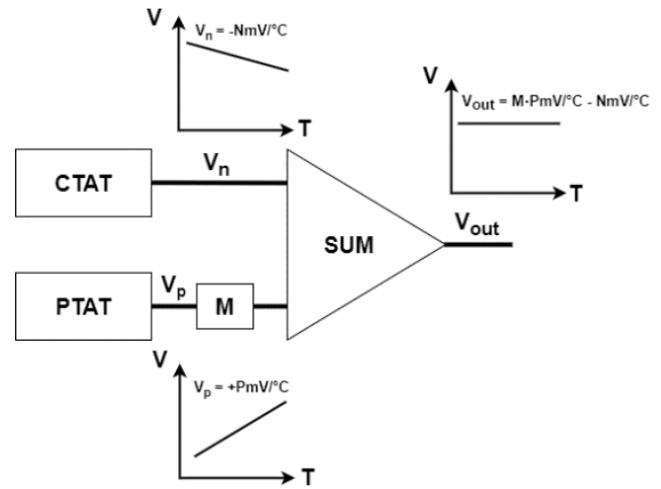


Fig.1. Voltage bandgap reference circuit idea

In order to obtain a voltage or current independent of the influence of temperature variations it is necessary to build two circuits: one with a positive temperature coefficient (PTAT - proportional to absolute temperature), i.e. one where, as the temperature increases, the value of the voltage or current output from the circuit will increase, and a circuit with a negative temperature coefficient (CTAT - complementary to absolute temperature). Then, as the CTAT and PTAT values will not be equal (because different circuits, e.g. a diode and a bipolar transistor, can be used to obtain positive and negative temperature coefficients), it is necessary to use an appropriate multiplier (block  $\cdot M$  at the Fig. 1) by which the absolute values can be made equal. The final step is to sum the output voltages or currents from the CTAT and PTAT blocks after applying mentioned  $N$ -multiplication, which should allow a reference value that is much less susceptible to changes due to temperature variations. Summing can be performed on operational amplifier circuit.

The abovementioned description could also be presented using mathematical formalism, i.e. assuming that  $V_{CTAT}$  is voltage from CTAT block,  $V_{PTAT}$  is voltage from PTAT block,  $M$  is scaling factor, and  $V_{SUM}$  is output of summing block, it is possible to provide  $V_{SUM}$  as:

$$V_{SUM}(T) = V_{CTAT}(T) + M \cdot V_{PTAT}(T)$$

After differentiating above equation by temperature the new equation can be given that shows common temperature relation of the used voltage sources:

$$\frac{\partial V_{SUM}(T)}{\partial T} = \frac{\partial V_{CTAT}(T)}{\partial T} + M \cdot \frac{\partial V_{PTAT}(T)}{\partial T}$$

Knowing that  $(\partial V_{CTAT}(T))/\partial T < 0$  and  $(\partial V_{PTAT}(T))/\partial T > 0$ , and having in mind that the aim is to get  $(\partial V_{SUM}(T))/\partial T = 0$  the M value for the smallest possible output temperature coefficient can be found:

$$\frac{\partial V_{CTAT}(T)}{\partial T} = -M \cdot \frac{\partial V_{PTAT}(T)}{\partial T}$$

which clearly shows that scaling  $V_{PTAT}$  value with the use of M multiplier block is crucial to minimise temperature variation of reference voltage.

In practice, however, it is only possible to achieve such an effect for very close range around one temperature, and for the others the resulting temperature coefficient remains non-zero (but very close to). This is because temperature coefficients also have their temperature coefficients of higher orders causing non-linearity, which cannot be removed by using such simple operations as addition and multiplication. This effect is called curvature error. As a result, the resulting temperature coefficient will be non-constant function of a curved (paraboloid) shape (see Fig. 2).

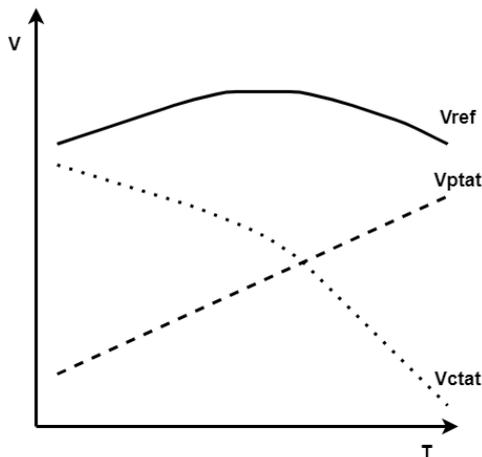


Fig.2. Example voltage waveforms at the output of CTAT and PTAT blocks with the resulting reference voltage

### III. DYNAMIC THRESHOLD MOS TRANSISTORS

The one of the most popular solutions adapted in the voltage/current references is the usage of bipolar junction transistors (BJT) that in a given configuration may play a role of positive and negative coefficient voltage source. The main advantage of using BJTs is that the reference circuit depends on physical constants and much less on the process however the BJTs downsides are large area occupation and design restrictions whenever pure CMOS process is used. A possible alternative proposed by [8], [9], [10] is to use DTMOS transistor

which is a special type of MOS transistor, i.e. it is created by connecting MOS transistor's gate to its substrate. Analysing the silicon cross section of DTMOS structure shown in Fig. 3, it is

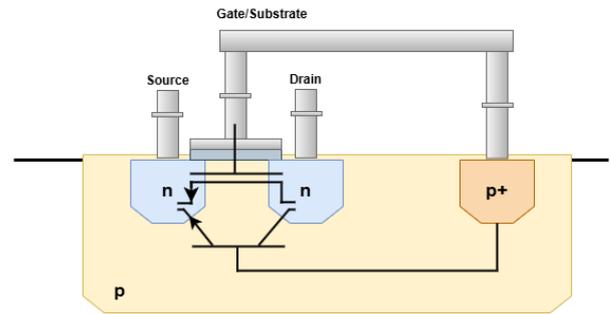


Fig.3. N-type Dynamic Threshold MOS transistor structure cross section

possible to identify this device as parallel connection of BJT and MOS transistors.

Thanks to that configuration the DTMOS's threshold voltage  $V_T$  changes dynamically, i.e. when the gate voltage increase effective threshold voltage falls resulting in transistor's current increase lowering the gate voltage (if transistor is biased via resistor connected to the supply voltage). Importantly, thanks to that configuration the operation voltage of the DTMOS transistor may be very low making it a good choice to applications working with very low supply voltages.

The payoff that must be fulfilled when it is decided to use DTMOS instead of classical MOS transistors is the fact that this device needs deep wells so naturally it will consume more space on layout (however still less when compared to BJT transistors).

Also building precise reference source based on this type of transistor is more difficult compared to a solution based on BJTs due to slightly higher process mismatches especially severe in weak inversion region. On the other hand using DTMOS transistors will provide homogeneity of transistors used in circuit which may provide overall benefit to circuit design. Schematic symbols of complementary DTMOS transistors are shown in Fig.4.

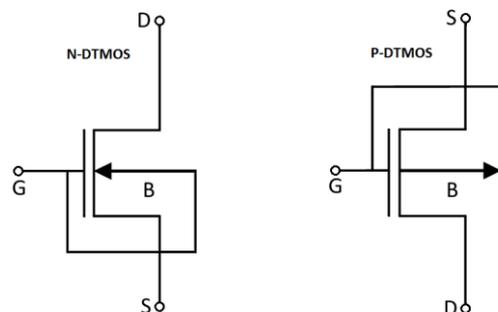


Fig.4. n-DTMOS and p-DTMOS schematic symbols

### IV. TEMPERATURE COEFFICIENT COMPARISON OF BJT AND DTMOS DEVICES

Referring to the principles of operation of the system (described in more detail in Chapter II), a current or voltage summed by an operational amplifier with a constant temperature coefficient  $\alpha$  (as far as possible not varying with temperature) is

an indispensable factor ensuring its stable operation, so that the reference current or voltage at the system output can remain constant i.e. the effect of temperature can be compensated.

In order to ensure that PTAT and CTAT temperature coefficients are less susceptible to temperature, it is necessary to select appropriate components forming PTAT and CTAT subcircuits.

In preparation for the construction of the bandgap reference circuit, there was performed a comparison of the temperature coefficient variation of BJT and DTMOS. This simulations were conducted for different current densities and transistor dimensioning - in the case of BJT transistors, these are the three sizes offered by the technology node, while in the case of DTMOS transistors, these are the proposed dimensions that should offer stable circuit performance.

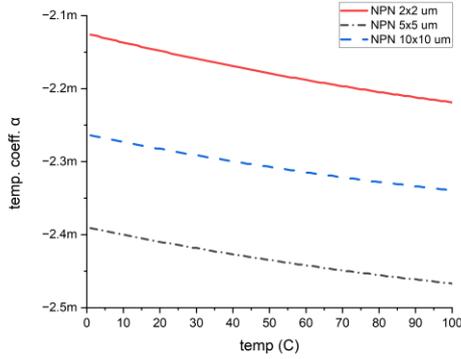


Fig.5. Temperature coefficients of different size NPN BJT transistors with constant current of 10 nA as a function of temperature

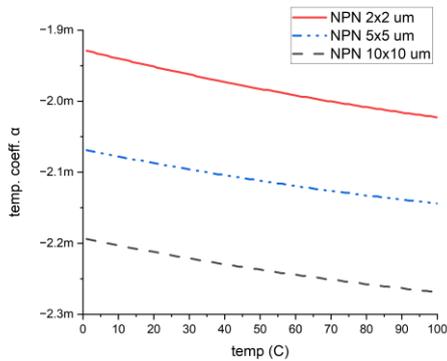


Fig.6. Temperature coefficients of different size NPN BJT transistors with constant current of 100 nA as a function of temperature

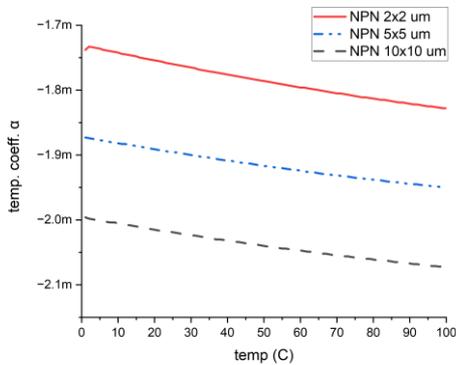


Fig.7. Temperature coefficients of different size NPN BJT transistors with constant current of 1 μA as a function of temperature

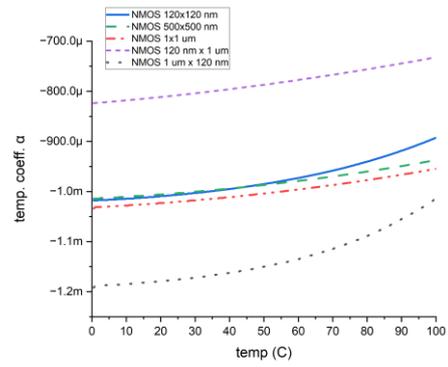


Fig.8. Temperature coefficients of different size n-type DTMOS transistors with constant current of 10 nA as a function of temperature

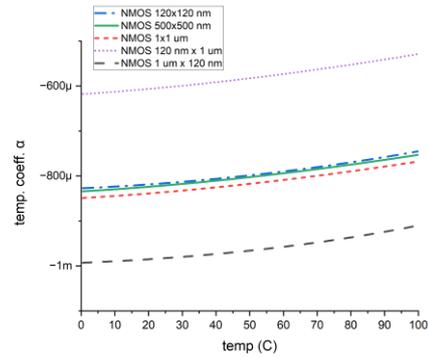


Fig.9. Temperature coefficients of different size n-type DTMOS transistors with constant current of 100 nA as a function of temperature

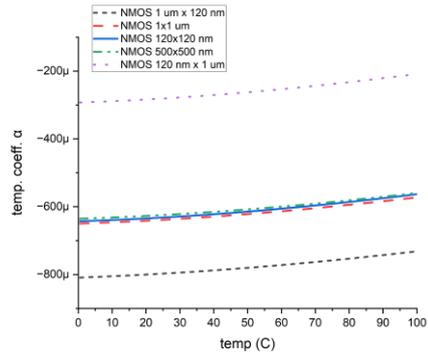


Fig.10. Temperature coefficients of different size n-type BJT transistors with constant current of 1 μA as a function of temperature

TABLE I  
TEMPERATURE COEFFICIENT OF BJT AND DTMOS DEVICES WITH A CURRENT OF 10 NA

Type	Size	$\alpha(0^{\circ}\text{C})$ mV/°C	$\alpha(27^{\circ}\text{C})$ mV/°C	$\alpha(100^{\circ}\text{C})$ mV/°C	$\Delta\alpha$ (0-100°C) mV/°C
NPN	2x2 μm	-2.219	-2.156	-2.126	-0.093
	5x5 μm	-2.339	-2.289	-2.266	-0.074
	10x10 μm	-2.467	-2.416	-2.391	-0.076
n-type DTMOS	120x120 nm	-1.018	-1.005	-0.893	0.124
	500x500 nm	-1.014	-1.002	-0.937	0.076
	1x1 μm	-1.033	-1.019	-0.954	0.077
	1μm x 120nm	-1.190	-1.174	-1.015	0.174
	120nm x 1μm	-0.849	-0.835	-0.771	0.078

TABLE II  
TEMPERATURE COEFFICIENT OF BJT AND DTMOS DEVICES WITH A CURRENT OF 100 nA

Type	Size	$\alpha(0^\circ\text{C})$ mV/°C	$\alpha(27^\circ\text{C})$ mV/°C	$\alpha(100^\circ\text{C})$ mV/°C	$\Delta\alpha$ (0-100°C) mV/°C
NPN	2x2 $\mu\text{m}$	-2.033	-1.954	-1.923	-0.110
	5x5 $\mu\text{m}$	-2.185	-2.104	-2.070	-0.115
	10x10 $\mu\text{m}$	-2.297	-2.220	-2.189	-0.108
n-type DTMOS	120x120 nm	-0.827	-0.814	-0.745	0.081
	500x500 nm	-0.834	-0.819	-0.753	0.080
	1x1 $\mu\text{m}$	-0.848	-0.834	-0.768	0.080
	1 $\mu\text{m}$ x 120nm	-0.992	-0.981	-0.910	0.082
	120nm x 1 $\mu\text{m}$	-0.656	-0.644	-0.582	0.074

TABLE III  
TEMPERATURE COEFFICIENT OF BJT AND DTMOS DEVICES WITH A CURRENT OF 1  $\mu\text{A}$

Type	Size	$\alpha(0^\circ\text{C})$ mV/°C	$\alpha(27^\circ\text{C})$ mV/°C	$\alpha(100^\circ\text{C})$ mV/°C	$\Delta\alpha$ (0-100°C) mV/°C
NPN	2x2 $\mu\text{m}$	-1.831	-1.755	-1.725	-0.106
	5x5 $\mu\text{m}$	-1.985	-1.906	-1.872	-0.113
	10x10 $\mu\text{m}$	-2.097	-2.022	-1.991	-0.106
n-type DTMOS	120x120 nm	-0.642	-0.630	-0.563	0.079
	500x500 nm	-0.635	-0.623	-0.559	0.075
	1x1 $\mu\text{m}$	-0.649	-0.637	-0.572	0.076
	1 $\mu\text{m}$ x 120nm	-0.808	-0.795	-0.731	0.076
	120nm x 1 $\mu\text{m}$	-0.372	-0.366	-0.315	0.056

According to the simulation results (see. Table I, Table II, Table III, Figs. 5-10) BJT transistors have bigger (by value) temperature coefficient compared to DTMOS transistors but have significantly bigger variation of the coefficient value, that takes place with temperature change. Having in mind that its necessary to provide stable temperature coefficient we choose DTMOS to construct PTAT and CTAT in our system.

## V. CURRENT REFERENCE CIRCUIT

Having in mind adaptation of the reference circuit in one of our projects [5] – [7] we decided to design the current reference circuit as it is used there for generating precise control of digital to analog converters and biasing points of the analog part of the integrated circuit. The proposed bandgap current reference circuit using DTMOS transistors is presented in Fig. 11.

The operation of the current reference is supported by the operational amplifier that thanks to the negative feedback keeps its both inputs at the same voltage level (branches P and N). Thanks to the fact that, the DTMOS transistors DT0 – DT4 have the same dimensioning, PMOS P1-P2 transistors have the same dimensioning, resistors R1A and R1B are equal, and the number of DTMOS transistor is different for negative and positive inputs of the operational amplifier, the PTAT and CTAT currents flow through the R2 and R1A respectively.

The temperature coefficient of current reference  $I_{REF}$  in specified temperature range is defined as follows:

$$TC_{I_{REF}} = \frac{I_{REF\ MAX} - I_{REF\ MIN}}{(T_{MAX} - T_{MIN}) \cdot I_{REF}(27^\circ\text{C})} \cdot 10^6 \left[ \frac{\text{ppm}}{^\circ\text{C}} \right]$$

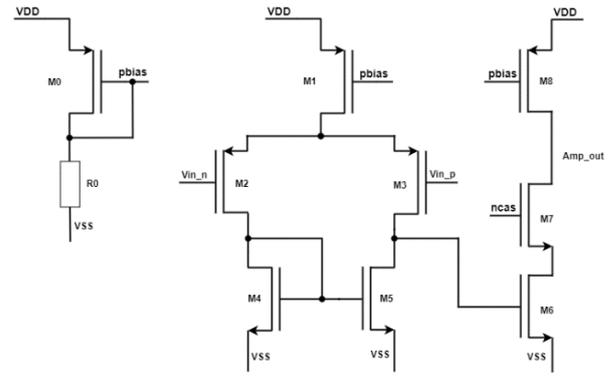
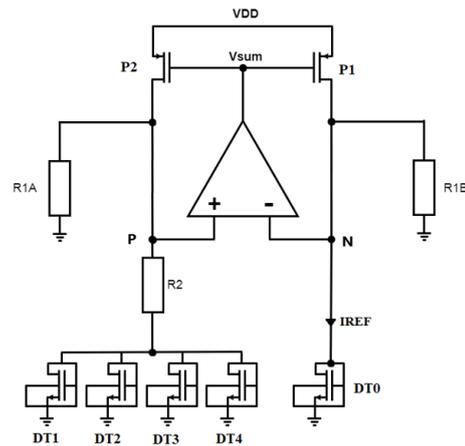


Fig.11. Bandgap current reference circuit based on DTMOS transistors

The operational amplifier used in the actual DTMOS transistor-based reference current system is based on a two-stage amplifier architecture, where the first stage is a simple differential pair with transistor based input, and the second stage is an amplifier built as a common-source circuit with a cascoded input transistor (see Fig. 12). The obtained voltage gain of the circuit is equal to 1795 V/V and the bandwidth is equal to 58 MHz (see Fig. 13) with consumption of 3.838  $\mu\text{A}$  current. Basic parameters of amplifier transistors are presented in Tab.4.



Schematic idea of the operational amplifier

Fig.12.

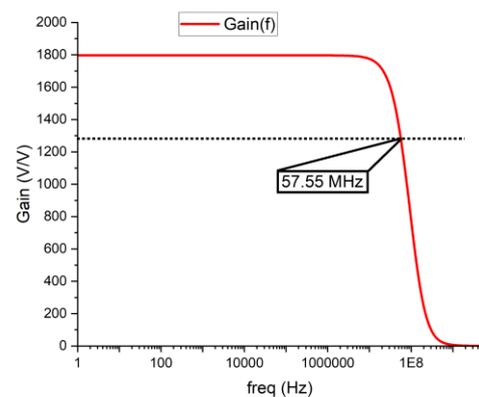


Fig.13. Amplifier gain in function of input signal frequency with pointed 3 dB cutoff value

TABLE IV  
BASIC PARAMETERS OF OPERATIONAL AMPLIFIER TRANSISTORS

Transistor	gm [ $\mu$ S]	rds [k $\Omega$ ]	ids [ $\mu$ A]
M1	22.827	168.211	1.403
M2	20.324	419.973	0.702
M3	20.299	483.803	0.701
M4	11.525	608.219	0.702
M5	11.512	599.891	0.701
M6	37.091	97.383	1.855
M7	39.464	111.584	1.855
M8	29.872	330.223	1.855

In the proposed current reference circuit, the standard resistors have been replaced with user-controlled resistor arrays, resistors, which saves space compared to the equivalent solution with parallel resistors (such resistors would have to have very high resistance values, which would result in a larger space occupied on the layout). Correction circuits allow the value of polarising resistors (R1A and R1B) to be changed by 50 k $\Omega$  (with a step of 12.5 k $\Omega$  from the basic value which is 1.6 M $\Omega$ ). Resistor R2 used to set the value of the divider, on which the temperature coefficient of the circuit mainly depends, allow change value by 20 k $\Omega$  (with a step of 5 k $\Omega$ ) from the basic value which is 441 k $\Omega$ .

Due to bandgap reference circuit high vulnerability to resistors value change, such a small change in resistor values allows even large variations induced by mismatches to be effectively minimised. Serially connected resistor circuit that is used to adjust temperature coefficient by dividing values summed on operational amplifier is more influential for the correct work of the entire bandgap circuit thus correction resistors that are switched have to be even smaller than the resistors used in load that biases bandgap circuit.

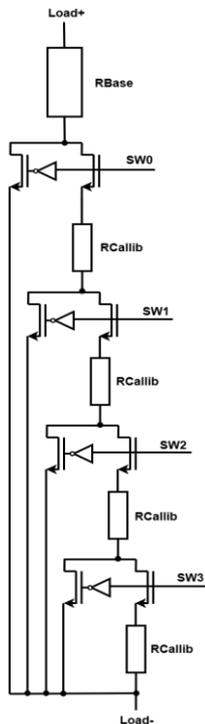


Fig.14. Adjustable resistor build on serial connected standard resistors that may be joined in chain-like sequence

Schematic of this adjustable resistor based on serial connected resistors is shown in the Fig. 14.

Transistors operating as current sources polarising the circuit, have been connected with two transistors allowing the construction of a topological mask based on a common centroid architecture. The DTMOS transistors have an additional keying (see Fig. 15) system allowing the selection of a bank of transistors (both in the N branch and in branch 1). Selected DTMOS dimensioning is 120 nm x 1  $\mu$ m. This size have the lowest temperature coefficient variation due to temperature change what is proven by simulation results in Tab.I, Tab.II and Tab.III.

Layout floorplan of the circuit is showed in Fig. 16.

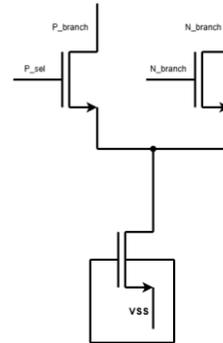


Fig.15. Schematic of DTMOS transistor cell with switchable input

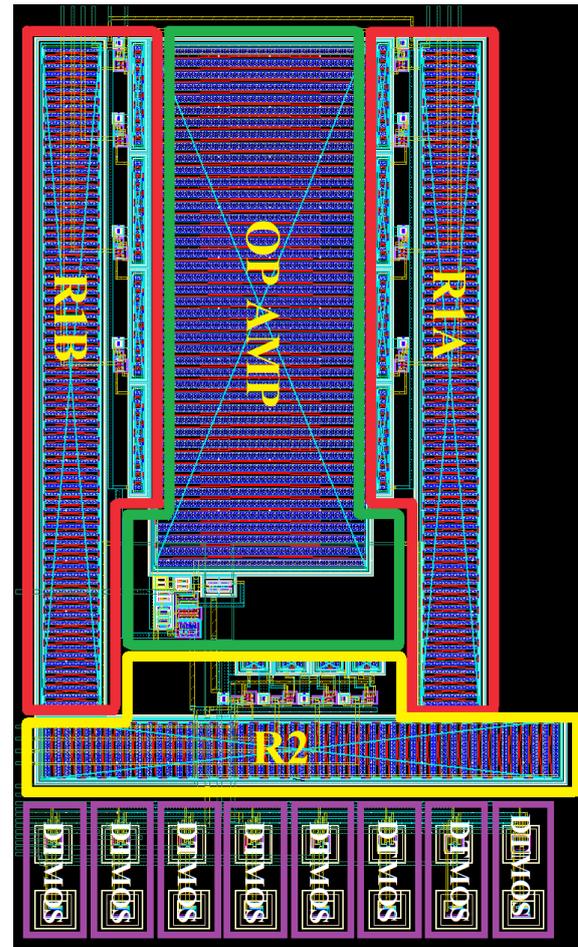


Fig 16. Floorplan of bandgap current reference circuit

## VI. SIMULATION RESULTS

The proposed circuit was designed in the CMOS 28nm process and its functionality was confirmed based on the postlayout simulations. The simulations show that circuit works properly, i.e. amplifier's output voltage compensates temperature influence by changing the PMOS current sources current resulting in current reference variation in the range of -340 nA to -339.4 nA (see Fig. 17), resulting in mean 18.87 ppm/(°C) temperature coefficient on entire temperature range (-20°C, 80°C) which was calculated with equation described before.

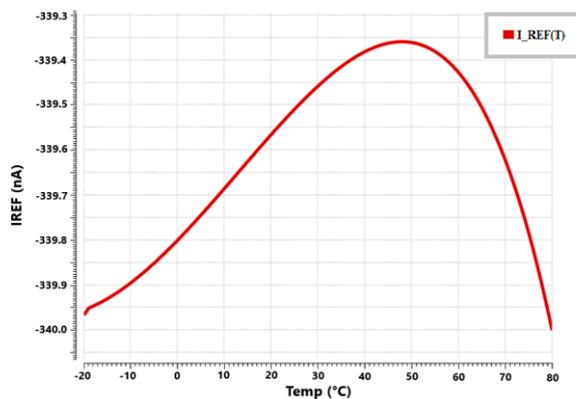


Fig.17. Reference current simulation results in terms of temperature variation

Simulation of circuit work also included Monte-Carlo simulations, that are useful to show possible mismatches that designed circuit may experience as a result of process nonidealities or design itself. Effects of these analysis are shown in Fig. 18 - resulted mean value of the current reference is equal to -324 nA with standard deviation equal to 84.4 nA. Histogram of this simulations shows that in some cases the values centers near value of -100 nA. Reason of that phenomenon is losing of the valid operating point, but it could be corrected by adjusting value of load circuits presented before. Importantly correction of the mismatches can be realized by the additional control of resistor banks R1A and R1B.

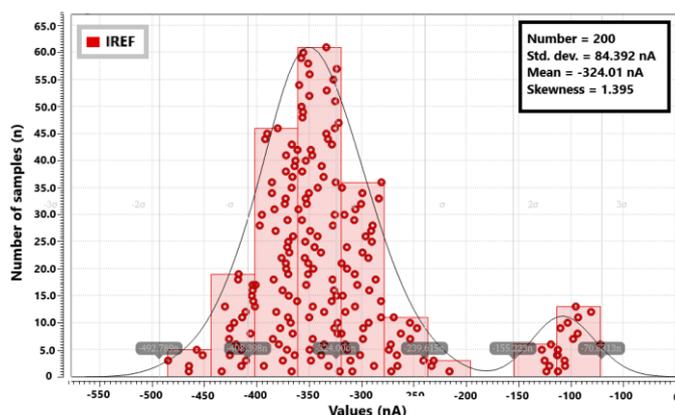


Fig.18. Monte-Carlo simulation result (200 runs) of current reference circuit working at 27°C temperature

The bandgap reference circuit discussed in this paper uses different techniques to minimize the effects of mismatch, among

which, in addition to passive techniques (which are good practices for creating a topological mask plan, that are the use of common centroid symmetry and the use of redundant transistors), active solutions based on adjustable value resistors have been used. By varying the value of the load circuits, the reference current can be changed as well as the temperature coefficient value can be minimized if its needed due to process mismatches.

The first and the most important correction mechanism are adjustable load circuits that allow user to change the value of load used to set current that flows through the branches of bandgap circuit and if necessary load that is used as voltage divider between branch 1 and N. Using serial resistor ladder (instead of parallel connected architecture that uses much more space due to necessity of using 2x times bigger resistors to maintain expected value) enables the opportunity to adjust effective resistance of load circuit by fixed step. This feature may be used to fix outliers that may be observed in Fig. 15. This values appears when due to mismatches operational amplifier drops from saturation region which cause drop of reference current, which could be corrected by re-adjusting load devices.

As also mentioned before DMTOS circuits are connected to switching transistors that allows to decide which transistors will be connected to N branch and which transistor will be connected to branch 1. By using this architecture its possible to make redundant DTMOS banks and choose the connection that provide best results (in layout floorplan at Fig. 13 are eight DTMOS banks, but effectively its connected 5 transistors at once – one to branch 1 and four to branch N to maintain 1:4 division, but its possible to make much bigger DTMOS banks reservoir). Introducing this architecture at this time provides opportunity to introduce more complex switching policy in the future (for example – Dynamic Element Matching).

## VII. CONCLUSIONS

Bandgap current reference circuit using DTMOS transistors to generate PTAT and CTAT voltage has been proposed.

This work confirms that DTMOS transistors could be effectively used to build homogenic bandgap reference circuit based only on MOS transistors. The proposed reference keeps its current stable against broad temperature range with much less area occupation when compared to BJT based references. We also presented the additional circuitry dedicated to mitigate downsides of DTMOS based references, i.e. their larger mismatches compared to BJT based reference.

## REFERENCES

- [1] Behzad Razavi. Design of analog CMOS integrated circuits. New York: McGraw-Hill, 2017.
- [2] B. Zhang et. al., „A 0.8V CMOS bandgap voltage reference design”. W: 2015 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC). 2015, s. 356–359
- [3] J. Jang iW. Shu. „A 5.6 ppm/C Temperature Coefficient, 87-dB PSRR, Sub-1-V Voltage Reference in 65-nm CMOS Exploiting the Zero- Temperature-Coefficient Point”. W: IEEE Journal of Solid-State Circuits 52.3 (2017).
- [4] Kok Chi-Wah and TamWing-Shan. CMOS voltage references: an analytical and practical perspective. Singapore: John Wiley, 2013.
- [5] P. Kmon, P. Maj, P. Grybos and R. Szczygiel, "An Effective Multilevel Offset Correction Technique for Single Photon Counting Pixel Detectors," in IEEE Transactions on Nuclear Science, vol. 63, no. 2, pp. 1194-1201, April 2016, <https://doi.org/10.1109/TNS.2016.2527834>

- [6] R. Kleczek, P. Kmon, P. Maj, R. Szczygiel, M. Zoladz and P. Grybos, "Single Photon Counting Readout IC With 44 e<sup>-</sup> rms ENC and 5.5 e<sup>-</sup> rms Offset Spread With Charge Sensitive Amplifier Active Feedback Discharge," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 70, no. 5, pp. 1882-1892, May 2023, <https://doi.org/10.1109/TCSI.2023.3241738>
- [7] P. Grybos et al., "SPHIRD–Single Photon Counting Pixel Readout ASIC With Pulse Pile-Up Compensation Methods," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3248-3252, Sept. 2023, <https://doi.org/10.1109/TCSII.2023.3267859>
- [8] A. -J. Annema, "Low-power bandgap references featuring DTMOSTs," in *IEEE Journal of Solid-State Circuits*, vol. 34, no. 7, pp. 949-955, July 1999, <https://doi.org/10.1109/4.772409>
- [9] S. Herbst. A Low-Noise Bandgap Voltage Reference Employing Dynamic Element Matching. Massachusetts, USA: Department of Electrical Engineering and Computer Science
- [10] Jianghua Chen, Xuewen Ni and Bangxian Mo, "A curvature compensated CMOS bandgap voltage reference for high precision applications," 2007 7th International Conference on ASIC, Guilin, China, 2007, pp. 510-513, <https://doi.org/10.1109/ICASIC.2007.44>