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A 5-dBm IIP3 3.5-mW LNA for 802.11ax Receiver in 40 nm CMOS

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***Abstract*—This article presents an inductively degenerated common-source low-noise amplifier (LNA) for a 5–6-GHz wireless local area network (LAN) receiver integrated circuit (IC). The LNA is equipped with gain-switching to prevent fast saturation in a presence of a large input signal. The simulated parameters, particularly the high linearity expressed in the input third-order intercept point (IIP3) of 5 dBm, make the design a promising solution for IEEE 802.11ax compliant receivers. Additionally, the low power consumption of 3.5 mW makes it suitable for portable devices.**

***Keywords*—low-noise amplifier (LNA), gain switching, inductive degeneration, 802.11ax, radio-frequency integrated circuit (RFIC)**

I. Introduction

Wireless communication systems, such as Wi-Fi and Bluetooth (BT) offer their users increasingly higher data rates. For example, IEEE 802.11ax (Wi-Fi 6 and Wi-Fi 6E) devices are capable of the physical layer (PHY) speed up to 9.6 Gbit/s under ideal conditions, i.e., the maximum channel bandwidth (BW) 160 MHz, 8×8 multiple input, multiple output (MIMO) implemented in both the transmitter (TX) and the receiver (RX), and possibly short distance between them to ensure low noise and distortion, thus enabling the highest possible modulation and coding scheme (MCS) [1], [2]. The IEEE 802.11ax standard introduces MCS10 and MCS11, employing 1024-QAM with coding rates of 3/4 and 5/6, respectively.

The 2.4 GHz industrial, scientific and medical (ISM) band technically allows for a 40 MHz channel width, but practically only 20 MHz is being used. Moreover, due to its unlicensed character, the band is very crowded, e.g., by BT and older Wi-Fi devices. Therefore, focusing on the 5 GHz (and 6 GHz) Wi-Fi band seems justified.

The privilege of using a wide channel exclusively, especially in the vicinity of other Wi-Fi users, is very rare. Instead, the channel is narrowed to 80 MHz or 40 MHz. Furthermore, the 8×8 MIMO, admittedly implemented in AC-powered devices, is virtually unavailable in battery-powered clients, as it would dramatically decrease battery life. The vast majority of modern portable Wi-Fi devices are provided with 2×2 (or sometimes 3×3) MIMO. Reducing both the channel width and the number of MIMO streams proportionally lowers the data rate. Therefore, the good sensitivity and linearity of the RX chain are important to maintain high MCS index and enable high PHY speed in low-power devices.

This article presents a design of a low-power highly linear low-noise amplifier (LNA) operating at 5 GHz for use in an IEEE 802.11ax compliant RX integrated circuit (IC).

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II. LNA Design

A. Design Requirements Analysis

A Wi-Fi receiver working at MCS11 must feature at least −43 dBm sensitivity, and −14 dB and +2 dB rejection levels for adjacent and alternate channel, respectively (or −17 dB and −1 dB for an 80 + 80 MHz channel bandwidth) [1]. However, as the distance between the RX and TX increases, and the signal power and quality decrease, the MCS index is lowered. Additionally, the channel width is reduced in the presence of interferers. The simplest modulation, i.e., BPSK (MCS0) combined with the narrowest channel (20 MHz) must be handled with a sensitivity P_S = −82 dBm. This imposes requirements on the noise level of the receiver. The RX's noise figure (NF) can be thus calculated as follows:

$$P_S = -174\,\text{dBm/Hz} + \text{NF} + 10\log(\text{BW}) + \text{SNR} \quad (1)$$

where: −174 dBm/Hz – thermal noise power density at 290 K, and SNR – signal-to-noise ratio.

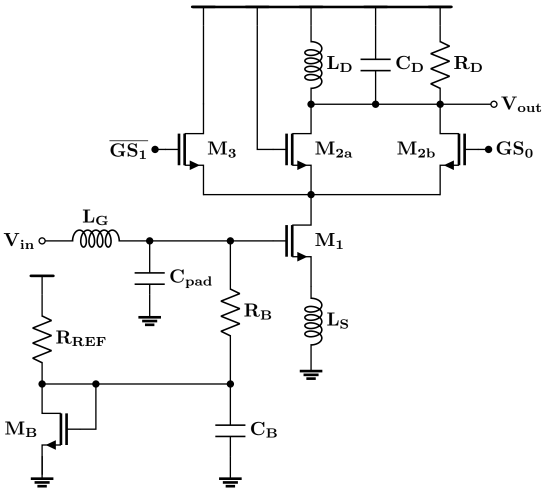
Equation (1) results in 49 dB for the sum of SNR + NF at 160 MHz MCS11 and 19 dB at 20 MHz MCS0. Leaving a sufficient SNR for the packet error rate (PER) of 10% [1], the RX's NF can be roughly estimated as 10 dB. However, most commercial products tend to lower the NF to achieve better sensitivity at higher data rates.

This value includes noise introduced by the antenna, filters, LNA, and subsequent stages. From the perspective of the IC, the LNA's NF remains crucial as it directly adds to the receiver total noise, according to (2) [3]:

$$\text{NF}_{\text{tot}} = 1 + (\text{NF}_{\text{LNA}} - 1) + \frac{(\text{NF}_2 - 1)}{G_{A,\text{LNA}}} + \frac{(\text{NF}_3 - 1)}{G_{A,\text{LNA}} \cdot G_{A,2}} + \cdots \quad (2)$$

where: NF_i – noise figure, and $G_{A,i}$ – available power gain of the i-th stage (e.g., mixer, amplifier, etc.).

The 802.11ax receiver must operate properly at a maximum input level of −30 dBm. Therefore, the RX chain should provide regulated gain from about 82 dB to 30 dB. Considering the peak-to-average ratio (PAR) of the OFDM signal (∼7.9)



M_1	99/0.04 µm/µm	C_D	260 fF
M_{2a}	56/0.04 µm/µm	C_B	900 fF
M_{2b}	43/0.04 µm/µm	C_{pad}	100 fF
M_3	25/0.04 µm/µm	C_{gs1}	50 fF
M_B	25/0.04 µm/µm	L_D	2.5 nH
R_D	1.3 kΩ	L_S	1.4 nH
R_B	10 kΩ	L_G	5.0 nH
R_{REF}	493 Ω		

Fig. 1. Cascoded CS LNA with inductive degeneration, biasing and gain switching

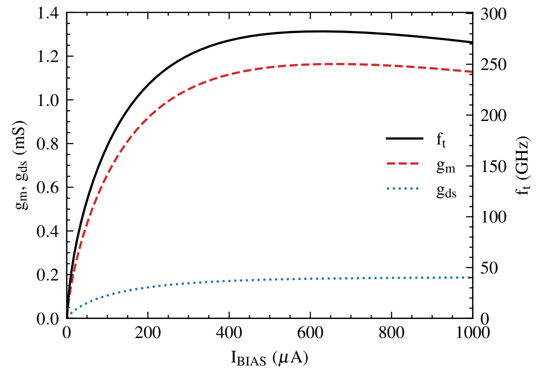


Fig. 2. Unit transistor's parameters in a function of bias current

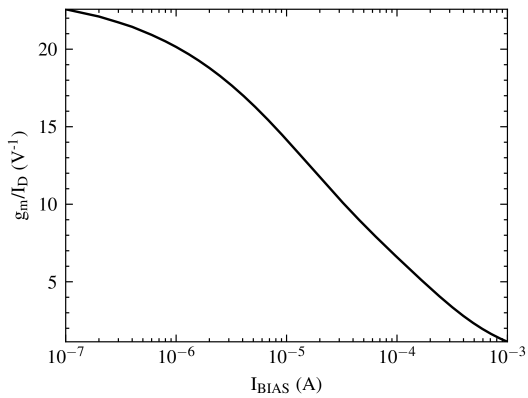


Fig. 3. g_m/I_D as a function of bias current

and possible envelope variations, the 1-dB compression point P_{1dB} should be set to about −20 dBm or higher. Along with compression, the intermodulation issue must also be considered. Since the RX must operate with signals up to −30 dBm with very dense modulation near other TXs occupying adjacent and further channels, it must demonstrate high immunity to the intermodulation. This can be expressed by a high value of the third-order intercept point (IP3).

B. Circuit Architecture

Common CMOS LNA architectures include the common-gate (CG) and common-source (CS), which can be single transistor or cascoded [4]–[7]. The CG configuration features a purely resistive input impedance of $1/g_m$, which enables excellent input matching over a wide frequency range, albeit at the cost of a relatively high NF. In contrast, the CS architecture provides a lower NF, while the cascode reduces the impact of the load tank on the input impedance and improves stability. Additionally, to improve the input matching, the source of the input transistor can be degenerated [8]. In order to avoid fast saturation, initial gain switching can be implemented in the LNA. For this project, the inductive degeneration cascoded CS architecture with gain switching, shown in Fig. 1, has been chosen.

Since low-inductance packaging techniques (e.g., flip-chip) still remain an expensive option, this design assumes that the IC will be wire-bonded to a package or a PCB. For the simulations, an average bond quality factor $Q = 20$ has been assumed [9]–[11]. The pad capacitance C_{pad} was assumed to be 100 fF.

C. Transistor Biasing

Figure 2 shows simulated parameters of a unit transistor with $W/L = 1$ µm/40 nm. When biased at 80-90% of its maximum transconductance $g_{m,\max}$, the transistor provides nearly optimal current density (I_D/W) in terms of speed (parasitic capacitances) and power consumption [10]. The lowest NF can be achieved with the transistor biased at its maximum transit frequency f_t, however, this point tends to occur before the transconductance g_m achieves its peak [12]. On the other hand, linearity can be improved with a higher bias current, where charge carrier velocity saturates and g_m becomes flat, providing little improvement with rising power consumption [13]. The noise-linearity trade-off encourages to bias the transistor in weak to moderate inversion [4], [13]. Figure 3 presents the g_m/I_D curve of the analyzed transistor. Here, to achieve high linearity without excessive noise or power consumption, the transistor has been biased at $g_m/I_D = 10$ and scaled so as to not exceed 3.5 mW of power dissipation from a 1.1-V supply. The width $W_1 = 99$ µm and the bias current of 3 mA have been selected.

The current reference, composed of M_B and R_{REF}, consumes 1 mA. The reference voltage is connected to the gate of M_1 by resistor R_B, which reduces the impact of the diode-connected M_B on the LNA input matching. Additionally, capacitor C_B provides a low-impedance path to ground for noise coming from the reference.

D. Gain Control

The cascoding transistor M_2 has the same width as the input transistor M_1. However, it is decomposed into two instances (M_{2a} and M_{2b}) which, together with M_3, provide a switched gain, controlled by means of GS_{10}. This configuration allows minimizing excessive capacitance variations while switching on and off the cascoding transistors. To provide uniform 3-dB gain steps, the width of M_3 and the division ratio of M_2 have been initially derived from (3) and (4) and then adjusted through simulations [10].

$$1 + \frac{W_3}{W_{2a} + W_{2b}} = \sqrt{2} \tag{3}$$
$$1 + \frac{W_3}{W_{2a}} = 2 \tag{4}$$

E. Input and Output Matching

The source inductance, $L_S = 1.4\,\mathrm{nH}$ and gate inductance $L_G = 5\,\mathrm{nH}$ have been chosen to provide the matched resistance $R_0 = 50\,\Omega$ and cancel out the reactive component at the frequency of interest, according to (5) and (6). These inductances are assumed to be realized by wire bonds since they are inevitable at these points.

$$R_0 = \frac{g_{m1} L_S}{c_{gs1}} \cdot \left(\frac{c_{gs1}}{C_{\text{pad}} + c_{gs1}} \right)^2 \tag{5}$$

$$\omega (L_G + L_S) = \frac{1}{\omega \left(c_{gs1} + C_{\text{pad}} \right)} \tag{6}$$

where: c_{gs1} – gate-source capacitance of M_1.

The load tank is optimized for the 500-Ω mixer input exhibiting about 30 fF of input capacitance. The resistor $R_D = 1.3\,\mathrm{k}\Omega$ helps maintain relatively flat gain in the desired frequency range. Since the next stage will be implemented on the same IC, the inductor $L_D = 2.5\,\mathrm{nH}$ (with $Q = 15.5$) is realized on-chip. Therefore, it dominates the total area occupied by the circuit (Fig. 4).

III. Simulations

A. Stability

Stability of the amplifier was verified by two sets of stability factors, i.e., μ together with μ', and Kf along with $B1f$. As shown in Fig. 5, all the factors meet the stability criteria ($\mu > 1 \wedge \mu' > 1$ and $Kf > 1 \wedge B1f > 0$) in a wide frequency range, guaranteeing the circuit is unconditionally stable.

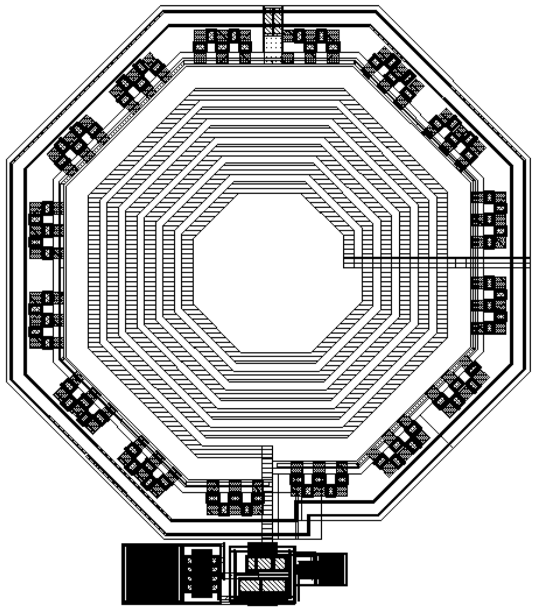


Fig. 4. Layout of the LNA building blocks

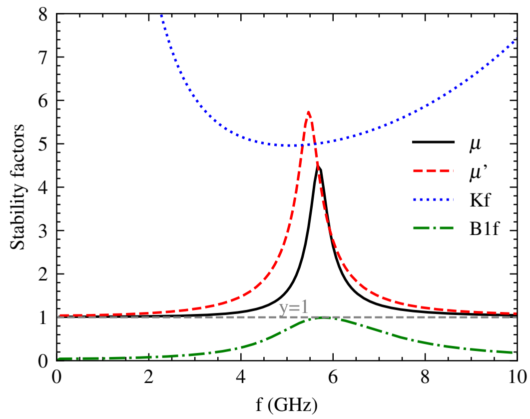


Fig. 5. Stability factors

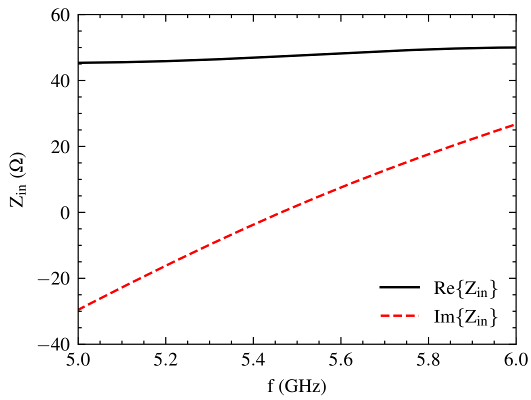


Fig. 6. Real and imaginary parts of the input impedance

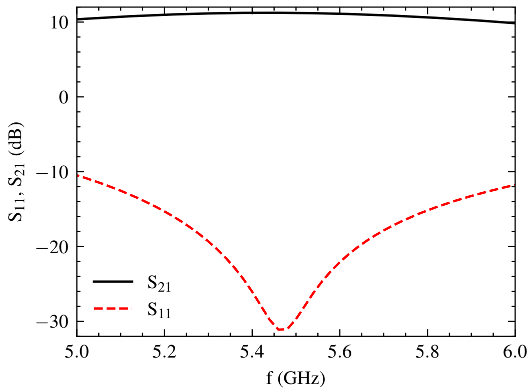


Fig. 7. Gain and input matching of the LNA

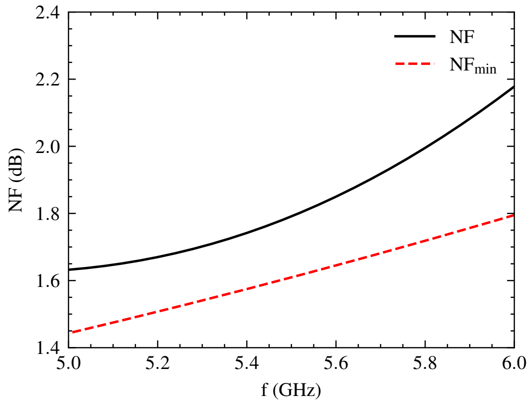


Fig. 8. Simulated and minimum noise figure

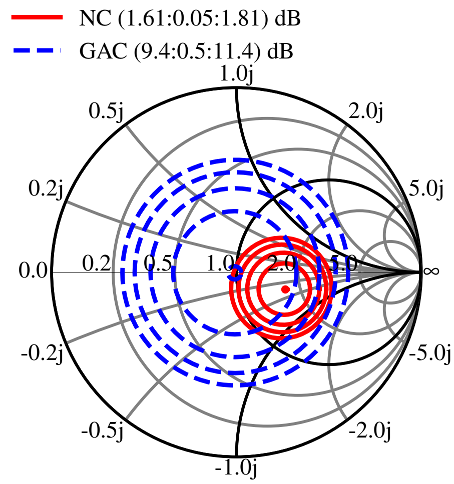


Fig. 9. Noise and available gain circles at 5.5 GHz

TABLE I
NOISE CONTRIBUTION SUMMARY OF THE LNA

Device	**Parameter**	**% of Total**
Input port	rn	56.78
M_1	id	10.48
L_G/r_s	rn	10.12
Output port	rn	4.46
M_1/r_b	rn	1.92
M_1/r_g	rn	1.41
M_1/r_{bod}	rn	1.14
M_{2a}	id	1.06
L_D/r_s	rn	0.95
M_{2b}	id	0.83

B. Input Matching and Gain

The input matching of the LNA has been designed to provide optimal power transfer of the weak RF signal from the antenna of $R_0 = 50\,\Omega$ to the input transistor. Figure 6 presents the real and imaginary parts of the LNA input impedance. At the center frequency 5.5 GHz $Re\{Z_{in}\} = 47.6\,\Omega$ and $Im\{Z_{in}\} = 2.0\,\Omega$.

The reflection coefficient and gain, expressed in S_{11} and S_{21}, were evaluated within the target frequency band. As shown in Fig. 7, the input is properly matched across the entire range, and the gain remains relatively flat, varying from 10.4 dB at 5.0 GHz to 11.2 dB at 5.5 GHz and decreasing slightly to 9.9 dB at 6.0 GHz.

C. Noise Analysis

As illustrated in Fig. 8, the noise figure of the designed LNA ranges from 1.63 dB at the lower end of the operating frequency range to 2.18 dB at the upper end. By modifying the input matching network, the NF could be lowered by an additional 0.2 dB, reaching the $\mathrm{NF_{min}}$. However, as results from the positions of the available gain and noise circles (Fig. 9), it would also degrade the gain by 0.5 dB.

The noise contributions were analyzed, and the ten most significant sources are summarized in Table I as percentages of the total integrated noise over the 1 kHz–10 GHz frequency range. The dominant contributions originate from the input port and the input transistor, confirming that the LNA design is properly optimized. A non-negligible contribution also arises from the parasitic resistance associated with the gate inductor L_G.

D. Gain Control

Next, the gain switching functionality was verified. The GS_{10} inputs were connected either to V_{DD} ($GS = 1$) or V_{SS} ($GS = 0$). According to the data presented in Fig. 10, the gain can be controlled from 6.7 dB to 11.2 dB. In the configuration $GS_{10} = 10$, both M_{2b} and M_3 are turned off. This situation is not optimal for the LNA and should be avoided. Notably, it provides a gain similar to $GS_{10} = 11$.

E. Linearity

The linearity of the proposed LNA was characterized through harmonic balance analysis. In the single-tone test, the input-referred 1-dB compression point P_{1dB} was determined to be -16.5 dBm. To further evaluate the intermodulation behavior, a two-tone test with a frequency spacing of 1 MHz was performed. As illustrated in Fig. 11, the LNA achieves the input third-order intercept point (IIP3) of 5.0 dBm.

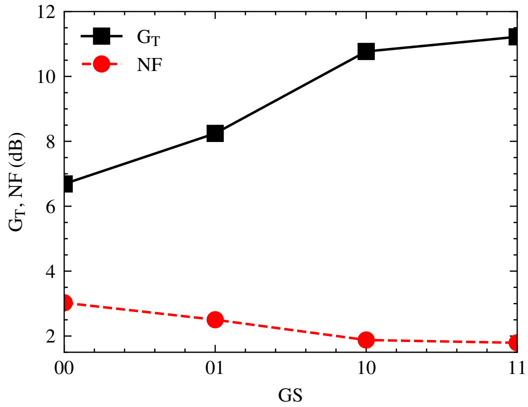


Fig. 10. Gain and noise in different gain-switching configurations

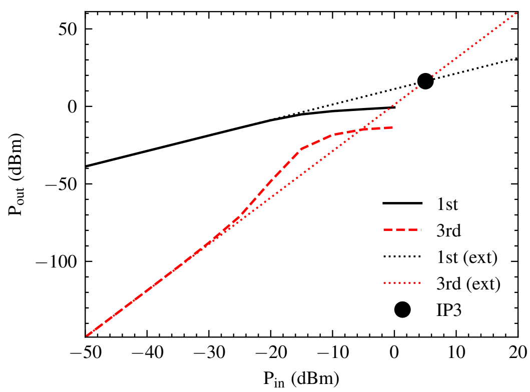


Fig. 11. IP1 and IP3 curves

F. Impact of the Bias Current

Finally, the amplifier was simulated under different bias conditions. Although increasing the bias current slightly improves the noise and gain performance (Fig. 12), the LNA provides the best linearity, expressed in IIP3 and P_{1dB}, at the initially selected 3 mA (Fig. 13).

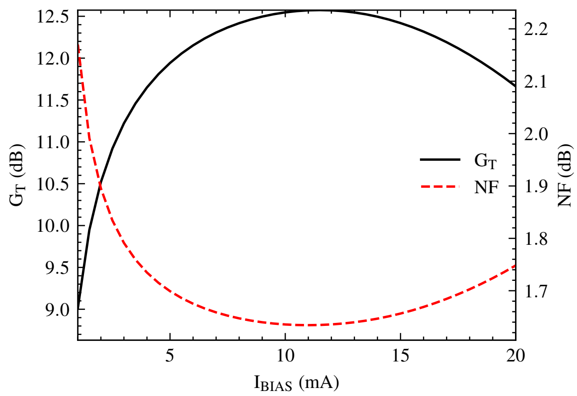


Fig. 12. Gain and noise at different bias currents

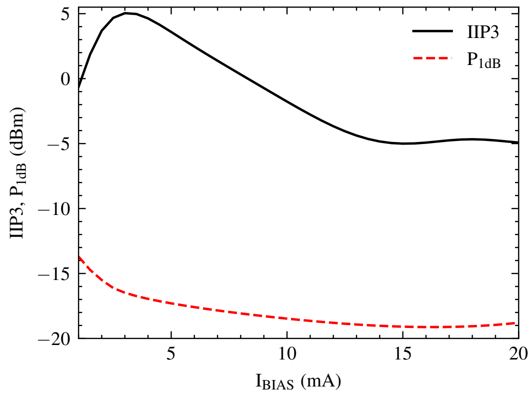


Fig. 13. Linearity of the LNA at different bias currents

G. Summary

The parameters of the designed LNA were collected and compared to similar CS LNA designs in Table II. The presented circuit offers good linearity while maintaining low power consumption. It also provides gain switching to improve linearity with a large input signal. The relatively high NF is mainly caused by the low-Q inductors, especially the relatively large gate inductor L_G. It should be noted that the other presented examples take advantage of the SOI technology, which allows for a significant reduction in noise via a floating body connection. The difference is especially noticeable in [5], where both types of body connections are reported.

TABLE II
COMPARISON WITH OTHER L-DEGENERATED CS LNAS.

Parameter	[4]	[6]	[5]	This work
Tech. [nm]	130 SOI	130 SOI	180 SOI	40
Freq. [GHz]	4.6–6	5–6	5	5–6
PDC [mW]	10	3	12	3.5
NF [dB]	0.6	0.65	0.95*/1.9**	1.77
IIP3 [dBm]	12	6	5*/6.5**	5
Gain [dB]	10.4	10.8	17.7	11.2
S11 [dB]	<−10	<−10	−33*/−22**	<−10.5
Gain control	No	No	No	Yes
Size [mm^2]	0.6024	0.6567	0.293	0.030***

* Floating-body transistors
** Body-contacted transistors
*** Estimated active area

IV. CONCLUSION

The inductively degenerated common-source low-noise amplifier design has been presented. The LNA is equipped with gain switching to prevent fast saturation when a large input signal is present. Its high linearity and other simulated parameters make the design a promising solution for the IEEE 802.11ax compliant receivers integrated circuits. Additionally, its low power consumption promotes the solution for application in portable devices.

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