INTL JOURNAL OF ELECTRONICS AND TELECOMMUNICATIONS, 2026, VOL. 72, NO. 2, PP. 1-9
Manuscript received November 14, 2025; revised April 2026. doi: 10.24425/ijet.2026.157936

Design and analysis of PTL based reversible logic encoder circuits for low-power applications

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***Abstract*—Gray codes are extensively used in modern digital systems to reduce errors occurring due to the sensitivity of binary transitions in communication and arithmetic circuits. This project discusses the design and implementation of a binary-to-Gray code converter using different XOR gate realizations and reversible logic gates to study performance and efficiency. Implementation of the converter using conventional XOR gates, XOR made from transmission gates (TG), Pass Transistor Logic (PTL) XOR, Feynman gate, Toffoli gate, and their PTL-based counterparts is presented. Synthesis and simulation for all designs are done using Cadence tools on 90 nm CMOS technology. Through comparative analysis, the implementations show that PTL-based Feynman gate implementation results in the least power dissipation, which is up to 90.15% lesser power consumption compared with the conventional XOR-based binary-to-gray code converter. The result implies that PTL and reversible logic represent an efficient alternative for low power and area-optimized design of digital circuits, suitable for modern VLSI applications.**

***Keywords*—Pass Transistor Logic (PTL); Transmission Gate; Reversible Logic; Feynman Gate; Toffoli Gate; Low-Power Code Converter**

I. INTRODUCTION

DIGITAL systems represent data using binary numbers, but many bits can change simultaneously while transiting from one binary value to another, sometimes causing transitional errors/glitches. Gray codes are used to overcome this problem because in Gray codes, only one bit changes at a time between
successive codes. Gray codes find wide applications in digital communication systems, rotary encoders, arithmetic circuits, and error correction due to this property.

The binary-to-Gray code conversion is done with XOR logic gates. Much of the efficiency of the conversion depends on the design and implementation of the XOR gates since they are those that determine the performance of the whole circuit in terms of power, speed, and area. Therefore, the optimization of XOR gate design is one of the major steps toward low-power and high-performance digital circuits.

This paper is on the design and implementation of a Binary to Gray Code Converter using different XOR gate realizations and reversible logic gates.

The designs include conventional XOR gates, XOR using transmission gates (TG), Pass Transistor Logic (PTL) XOR, Feynman gate, Toffoli gate, and Feynman and Toffoli gates using PTL based 3T XORs. Designs have been synthesized and simulated using Cadence tools with 90 nm CMOS technology in order to estimate their performance. The parameter-based power consumption, delay, and transistor count are compared for different implementations. The potential for reversible logic and PTL-based designs is explored in this work for the development of energy-efficient, compact circuits suitable for future applications in VLSI. The obtained design has significant power savings but with a slight increase in delay and transistor count, which makes it suitable for low-power IoT and portable devices.

II. LITERATURE REVIEW

The optimization of logic conversion and computation efficiency has been the main focus of recent developments in low-power digital circuit design. In contrast to traditional CMOS-based designs, Varshini and Siddeshwara Prasad [1] proposed a Binary to Gray code converter based on NAND-based XOR logic implemented in Cadence 180 nm CMOS technology, achieving better layout density and lower power consumption. Sharmila Devi [2] created a reversible carry-select adder based on MCML that showed notable power dissipation reductions while retaining a high processing speed, making it appropriate for DSP applications. Neeraja Bandi et al. [3] investigated a variety of logic-based gates and adders based on pass transistors, demonstrating better power and delay characteristics than their conventional CMOS counterparts. By demonstrating the viability of photonic logic circuits through temperature-dependent optical phase modulation at 10 kbps, Tian et al. [7] demonstrated an optical implementation of a Feynman gate using silicon micro ring resonators, achieving logic functionality. In order to determine the best gate structures, Batish et al. [8] examined reversible logic full adders and contrasted their hardware efficiency, garbage output, and quantum cost. Fault-tolerant CMOS logic circuits using preservative reversible gates were introduced by Parvin and Altun [9], improving fault detection and design testability. Khakpour et al. [10] developed compact, high-speed parity generators and code converters using Quantum-dot Cellular Automata (QCA) technology, achieving low-energy operation suitable for nanoscale systems. Tomar et al.

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[11] proposed a reversible D flip-flop that minimized garbage outputs and propagation delay, improving circuit efficiency. Sangeetha et al. [12] designed a reconfigurable reversible adder using Toffoli and BJN gates in Cadence with VHDL, resulting in a power reduction of approximately 2005 nW. Bari et al. [13] implemented a 4-bit binary-to-Gray converter integrated with an 8×4 barrel shifter using nanoscale MOS transistors, demonstrating high-speed and energy-efficient performance for communication and arithmetic operations. Haghparast and Navi [14] introduced a nanotechnology-based reversible full adder design optimized for minimal transistor count and low power consumption. Chiwande and Dakhole [15] proposed an efficient reversible logic multiplier aimed at reducing switching power in arithmetic circuits. Morrison et al. [4] extended reversible design principles to memory structures by developing static and dynamic RAM arrays that use reversible gates and decoders which significantly improved energy efficiency. Hirayama et al. [5] established theoretical limits for Toffoli-based reversible circuits. Their findings offered insights for optimizing gates. Thapliyal and Ranganathan [6] proposed efficient reversible sequential circuits that reduce quantum costs and garbage outputs. Finally, Landauer [16] laid the theoretical foundation for reversible computing proving that the loss of information in irreversible circuits results in heat generation, emphasizing the importance of energy preserving logic design.

This work develops a binary to gray code converter using 90 nm CMOS technology and reversible logic based on PTL implementation. The design aims to reduce power consumption, delay, and the number of transistors. It clearly shows the trend toward reversible and nanoscale logic for better circuit efficiency. The proposed model performs better than traditional CMOS methods and is well-suited for small, low-power VLSI systems.

III. Objectives

The main objectives of this project are:

- To design and implement a Binary to Gray Code Converter using various XOR logic styles.
- To realize XOR gates using Transmission Gate Logic and Pass Transistor Logic.
- To implement Binary to Gray Code Converter using Reversible logic gates.
- To simulate all designs using Cadence tools with 90 nm CMOS technology.
- Compare and analyze designs based on power, delay, and transistor count.
- To find the most efficient design for digital low-power applications.

IV. Code Converter

A. *Binary to Gray Code Converter*

A Binary to Gray Code Converter is a digital circuit that converts a binary number to its Gray code representation. In Gray code, consecutive numbers only differ by one bit. By having only one bit change between consecutive values, the Gray code resolves errors from multiple bits changing in a sequence and reduces error in applications such as mechanical encoders, analog to digital conversion (ADC), and communication systems, where minimizing the amount of errors due to changing bits is imperative for accurate application performance.

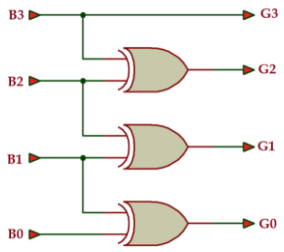


Fig.1. Binary to Gray Code converter using XOR gates

The Gray code of a binary number is generated by taking the most significant bit (MSB) of the Gray code to be the same the MSB of the binary number. Then, subsequent bits of the Gray code are generated using an XOR function as shown in Fig.1, between the current bit of the binary number and the previous bit of the binary number. This process ensures that adjacent values of the Gray code only differ by one bit, which minimizes errors in digital systems by decreasing the possibility of multiple bit transitions at once as shown in TABLE I.

TABLE I
TRUTH TABLE OF BINARY TO GRAY CODE CONVERTER

Natural-binary code				Gray code			
B3	B2	B1	B0	G3	G2	G1	G0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

V. Transmission Gate, Reversible Logic Gates & PTL

A. *Transmission Gate*

A Transmission Gate is a CMOS-based switch that allows the input signal to pass through to the output when the control signal is high, and blocks the signal when the control signal is low.

In the previous stage, a Binary to Gray code converter was designed using standard XOR gates. In this stage, the same converter is re-implemented using XOR gates constructed with transmission gate logic. The XOR gate built using this logic plays a crucial role in this implementation, and the circuit diagram is shown in Fig. 2.

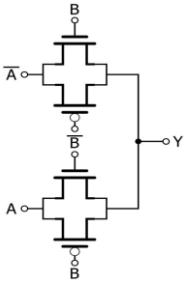
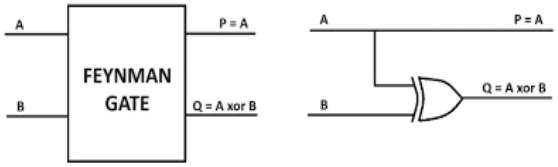


Fig.2. XOR gate using Transmission Gate Logic.

B. Reversible logic

Reversible logic refers to a type of digital circuit or logic gate with k-inputs and k-outputs, where the output uniquely determines the input, ensuring no information is lost. The unused output in such a gate is referred to as a "garbage output." These outputs, which are required solely to maintain the reversibility of the gate, are known as garbage outputs.

A Feynman gate is a 2×2 reversible logic gate that takes two inputs (A and B) and produces two outputs (P and Q), as illustrated in Fig. 3(a) and Fig. 3(b). The truth table for this gate is presented in TABLE II. It is also commonly referred to as the Controlled-NOT (CNOT) gate in the context of quantum computing.



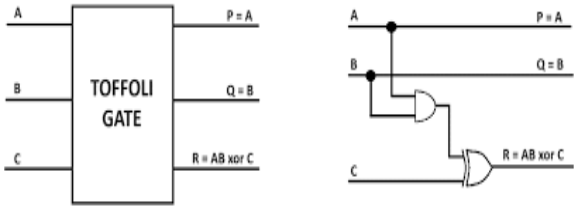
(a) (b)

Fig.3. Feynman Gate (a) Block Diagram (b) Schematic Representation

TABLE II
Truth table of Feynman Gate

Input		Output	
A	*B*	*P*	*Q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

A Toffoli gate is a 3×3 reversible logic gate.It takes 3 inputs (A, B, C) and produces 3 outputs (P, Q,R) as in Fig.4(a) and 4(b) and outputs represented in TABLE III. Also called the Controlled-Controlled-NOT (CCNOT) gate.



(a) (b)

Fig.4 Toffoli Gate (a) Block Diagram (b) Schematic Diagram

TABLE III
Truth table of Toffoli Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

C. Pass Transistor Logic(PTL)

The XOR gate can be implemented efficiently using PTL, which includes employing both NMOS and PMOS transistors as controlled switches to realize the logic. In this configuration, the logic levels are passed by the transistors directly from input to output with a minimum requirement of additional pull-up or pull-down networks ,hence the transistor count reduces, resulting in lower power consumption and faster switching speed compared to conventional CMOS implementations as shown in Fig.5 PTL circuit is designed.

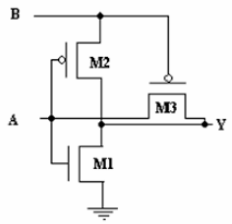


Fig.5. Circuit Diagram of XOR Gate Using Pass Transistor Logic (PTL)

VI. Design of Binary to Gray Code Converters Reversible Logic Gates

A. Binary to gray code convertor using Feynman Gate

The implementation of a Binary to Gray code converter using Feynman gates, which are 2×2 reversible logic gates, is shown in Fig. 6. The Feynman gate is particularly effective for performing the XOR operation, which is crucial in the process of generating Gray code. The most significant bit (MSB) of the Gray code is identical to the MSB of the binary input. Each subsequent Gray bit is generated by performing an XOR operation between two adjacent binary bits.

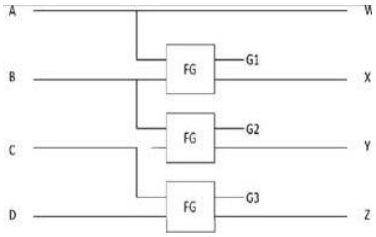


Fig.6. Design of Binary to Gray Code Converter using Feynman Gate

B. Binary to gray code convertor using Toffoli Gate

The given circuit diagram represents a 4-bit Binary to Gray code converter implemented using Toffoli Gates (TG) as shown in Fig.7

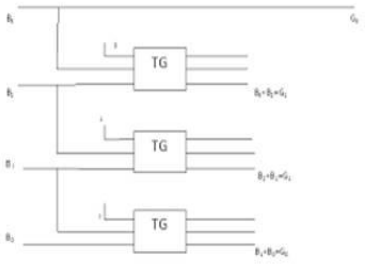


Fig.7. Design of Binary to Gray Code Converter using Toffoli Gate.

VII. Implementation of Required Basic Gates

Feynman Gate

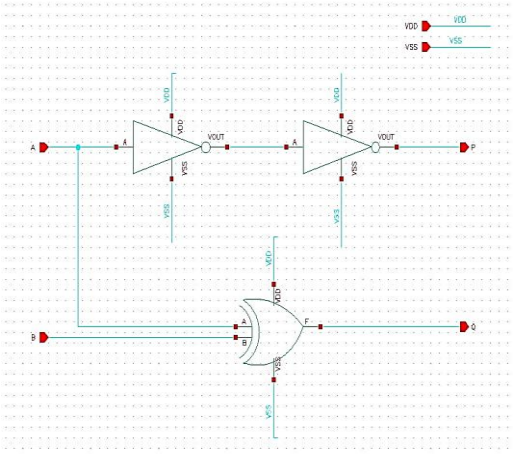


Fig.8. Schematic of Feynman Gate

The schematic of a Feynman gate (also known as a Controlled NOT gate or CNOT gate) as shown in Fig.8 is a 2×2 reversible logic gate with two inputs (A, B) and two outputs (P, Q) defined as: P = A, Q = A ⊕ B.

In the design of the Feynman gate, input A is directly transferred to the output without any logic modification. However, in Cadence Virtuoso, direct connections may cause floating nodes or unstable outputs. To ensure proper signal drive and stable simulation, an inverter pair (buffer) is used to pass A while maintaining its original logic level, thereby preserving circuit functionality and improving simulation accuracy. While the second output performs an XOR operation between A and B. The Feynman gate is widely used for fan-out operations in reversible circuits, serving as a building block for reversible computing and quantum logic systems. It helps minimize energy loss as it adheres to reversible logic principles.

A. Toffoli Gate

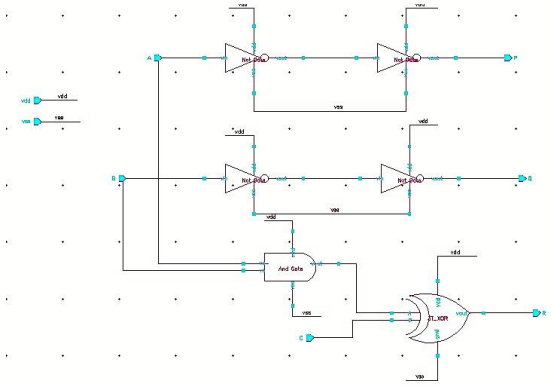


Fig .9. Schematic of Toffoli Gate

The schematic of a Toffoli gate as shown in Fig.9 is a 3×3 reversible logic gate with inputs A, B, and C, and outputs P, Q, and R, defined as: P = A, Q = B, R = AB ⊕ C.

The circuit is built using a combination of logic gates such as AND & XOR. The Toffoli gate acts as a universal reversible gate, capable of implementing any Boolean function without loss of information. In this schematic, NOT gates are used to generate signal inversions, while AND & XOR gates generate the required output function.

B. 3T XOR Using PTL Logic

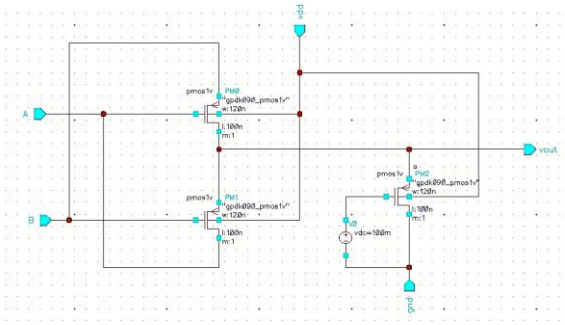


Fig.10. Schematic of XOR gate using 3T

The given schematic in Fig.10. shows a 3-transistor XOR gate implemented using Pass Transistor Logic (PTL). It realizes the XOR operation equation 1.

$$Vout = A \oplus B = A \cdot \bar{B} + \bar{A} \cdot B \qquad (1)$$

The PMOS transistor connects between VDD and the output and is controlled by B, while the NMOS transistors act as switches driven by A and B to transfer the required logic levels. When B is low, the PMOS conducts, and the output follows A; when B is high, the NMOS path conducts, and the output becomes the inverse of A. This behavior ensures that the output is logic high when A and B are different and logic low when they are the same, which defines XOR. The design is highly efficient in terms of transistor count, power, and delay, making it suitable for compact and low-power circuits, though it can experience minor voltage loss when NMOS transmits logic '1'.

VIII. Proposed Methodology of Circuit

A. Design of Binary to Gray Code Converter using Conventional XOR gates

In the theoretical design of the Binary to Gray Code Converter, the most significant bit (MSB) of the binary input is directly passed to the corresponding MSB of the Gray code output, as no logic operation is required for this bit. However, in practical implementation using Cadence Virtuoso, directly connecting the input to the output without a driving element can cause simulation issues, such as floating nodes or improper waveform behavior. This is because Virtuoso requires all output nodes to be explicitly driven to ensure proper signal integrity and drive strength. To address this, an inverter pair (i.e., a buffer) as shown in Fig.11 was introduced to pass the MSB without altering its logic level. This ensures accurate simulation results while preserving the intended functionality of the circuit.

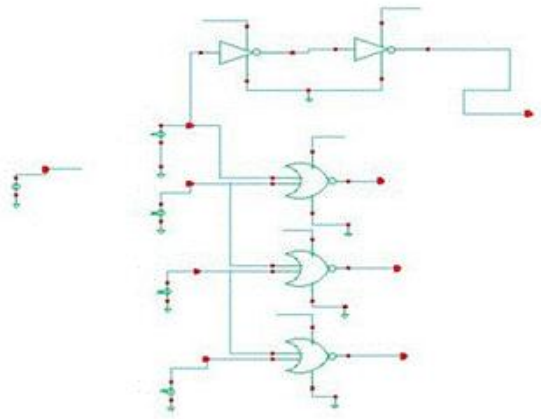


Fig.11. Schematic Representation of Binary to Gray Code Converter implemented using Conventional XOR gates.

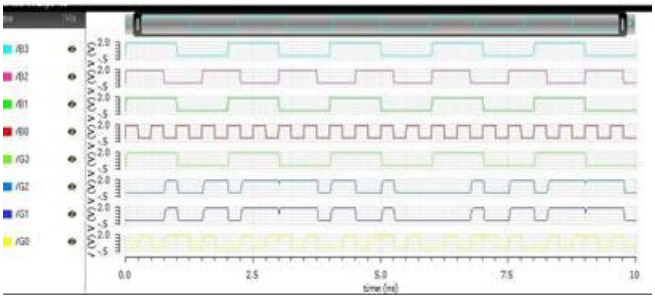


Fig.12. Transient response of Binary to Gray Code Converter implemented using conventional XOR gate.

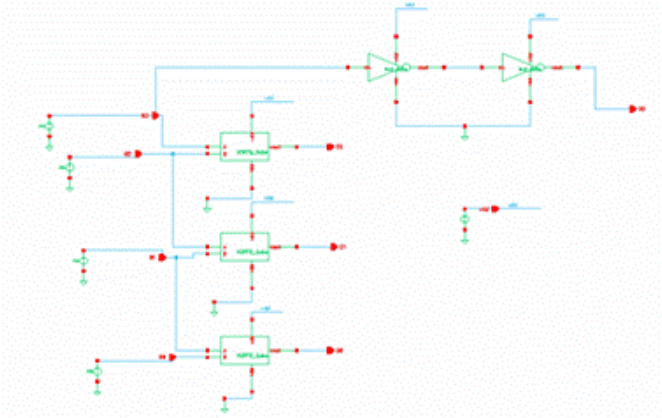


Fig.13. Schematic Representation of Binary to Gray Code Converter using Transmission XOR gates.

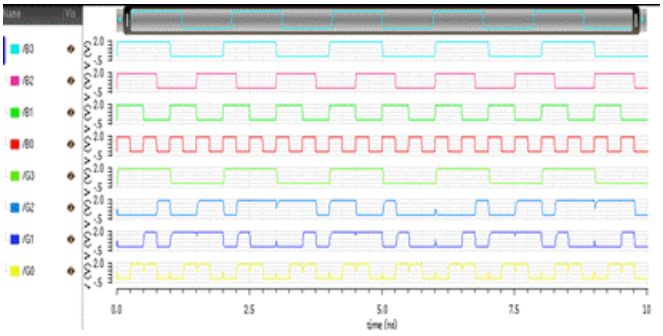


Fig.14. Transient response of Binary to Gray Code Converter implemented using Transmission XOR gate.

The waveform as shown in Fig.12 confirms the correct operation of the design, with each binary input accurately converted into its corresponding Gray code. The transitions observed in the output waveform match the expected behavior, validating both the functionality and correctness of the implemented logic circuit.

B. Design of Binary to Gray Code Converter by Replacing Conventional XOR gates with Transmission XOR gates

This design uses complementary transmission gates (PMOS and NMOS transistors) to create a transmission gate-based XOR (TXOR) gate in place of each conventional XOR gate. To guarantee appropriate drive strength and signal integrity during simulation in Cadence Virtuoso, the MSB is routed to the output via a buffer. TXOR gates are used between neighboring binary input bits to generate the remaining Gray code bits. In comparison to conventional CMOS-based XOR gates, this implementation optimizes transistor-level design by lowering power consumption and area while maintaining the same logical functionality.

The circuit, as implemented in Fig. 13, demonstrates correct functionality, as evident from the waveform output in Fig. 14. For each binary input, the corresponding Gray code output is accurately generated, and the signal transitions in the waveform align with the expected behavior.This confirms that the transmission gate-based XOR implementation operates reliably and accurately within the Binary to Gray Code Converter design.

C. Design of Binary to Gray Code Converter with Toffoli Gates

The design employs multiple Toffoli gates, known as universal gates in reversible logic, to perform the XOR operations necessary for Gray code generation. The implementation is shown in Fig.15. A buffer is used to directly pass the most significant bit (MSB) from the input to the output without alteration. The 4-bit binary inputs are processed through the Toffoli gates, which, by leveraging a constant logic high control line, function effectively as controlled-NOT gates to realize XOR operations. This implementation highlights the versatility of Toffoli gates in constructing reversible logic circuits for efficient binary to Gray code conversion.

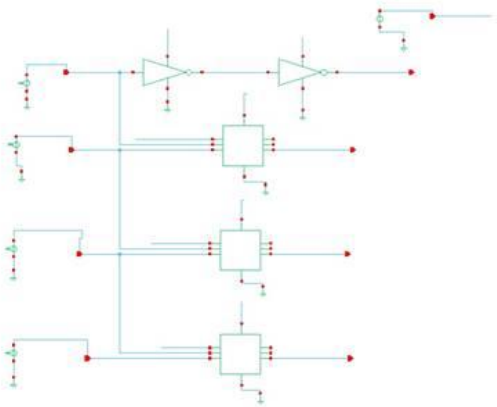


Fig.15. Schematic Representation of Binary to Gray Code Converter using Toffoli gates.

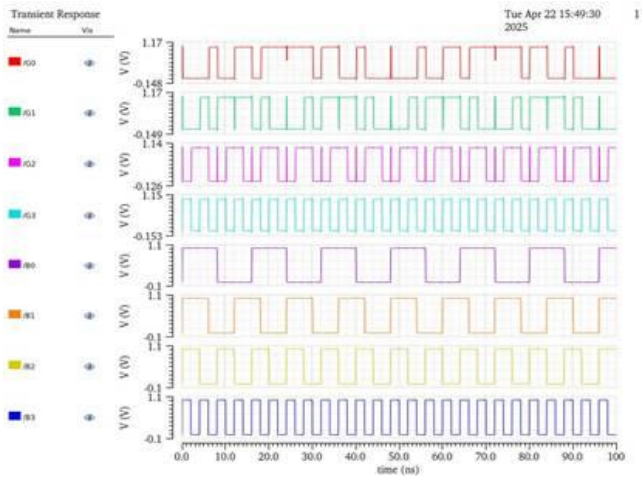


Fig.16. Transient response of Binary to Gray code converter implemented using Toffoli gate.

The transient response simulation output of the 4-bit Binary to Gray code converter, implemented using Toffoli gates as shown in Fig. 16, was evaluated and yielded accurate results, as presented above.

D. Design of Binary to Gray Code Converter with Feynman Gates

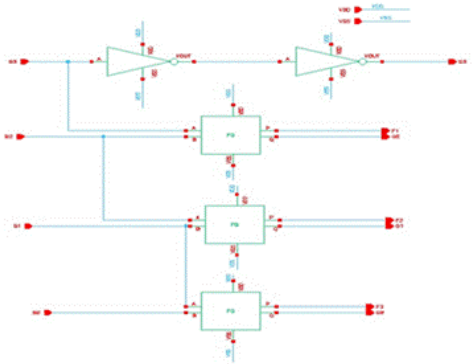


Fig.17. Schematic Representation of Binary to Gray Code Converter using Feynman gates.

The design utilizes three Feynman gates to perform the XOR operations required for Gray code generation. Additionally, a buffer is employed to directly transfer the most significant bit (MSB) without modification as shown in Fig.17. The input lines represent the 4-bit binary number, while the output lines produce the corresponding Gray code.

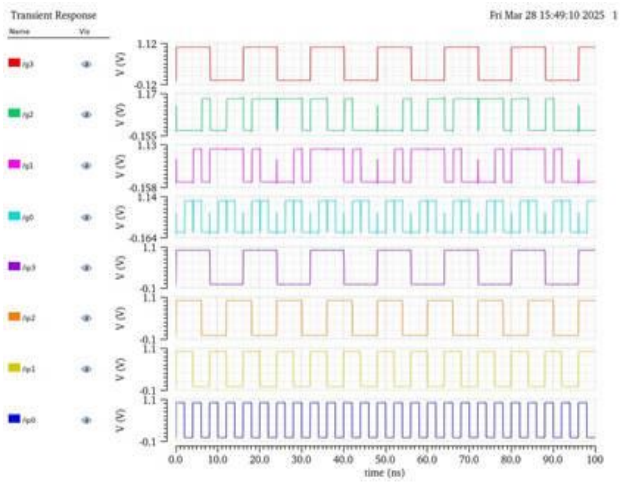


Fig.18. Transient response of Binary to Gray code converter implemented using Feynman gates.

The simulation confirms that the circuit accurately performs the intended Binary to Gray code conversion as shown in Fig.18. The design ensures efficient hardware utilization while maintaining reversibility. The use of Feynman gates contributes to low quantum cost, minimizes unnecessary garbage outputs, and makes the design well-suited for low-power and quantum-based systems.

These logical transformations are achieved using Feynman gates, which are reversible and capable of executing XOR operations with minimal hardware and energy consumption. Their reversible nature ensures no loss of information during computation a critical requirement in reversible logic and quantum computing.

IX. Implementation Using Pass Transistor Logic (PTL)

Pass Transistor Logic (PTL) is an efficient design technique used to reduce the number of transistors and overall power consumption in digital circuits. Unlike conventional CMOS logic, PTL uses the capability of transistors to pass logic levels directly between nodes, thereby minimizing switching activity and reducing area. In this project, PTL is employed to redesign the XOR gate and further used to implement Feynman and Toffoli gates for the Binary to Gray Code Converter.

Since the schematic structure of the Binary to Gray Code Converter remains the same as in the non-PTL implementations, the key difference lies in the internal transistor-level realization of XOR gates. Hence, this section focuses on the simulation results and transient responses obtained from PTL-based implementations.

A. Binary to Gray Code Converter Using PTL XOR Gate

In this design, the XOR gates within the converter are replaced by PTL-based XOR circuits. The PTL XOR design uses fewer transistors compared to conventional CMOS or transmission gate logic, which leads to lower power dissipation and faster switching. The functional correctness of the converter is verified using transient analysis in Cadence under 90 nm CMOS technology.

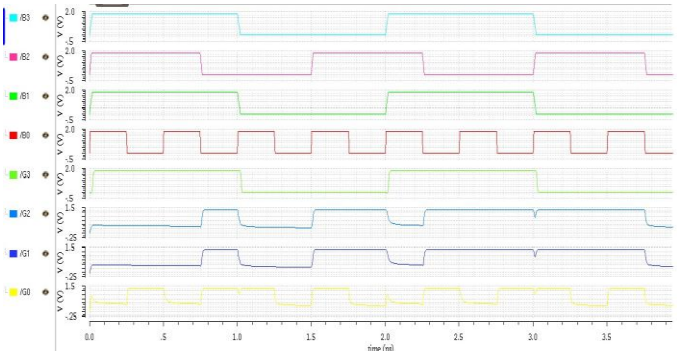


Fig.19. **T**ransient response of Binary to Gray Code Converter implemented using PTL XOR gate.

The transient waveform as shown in Fig.19 confirms accurate Binary to Gray code conversion while exhibiting reduced propagation delay and power consumption compared to the conventional XOR-based design.

B. Binary to Gray Code Converter Using Toffoli Gate with PTL based XOR

The Toffoli gate is a 3×3 reversible logic gate used to realize complex logic functions. Replacing its internal XOR logic with PTL-based XOR gates reduces both transistor count and energy consumption while maintaining logical accuracy.

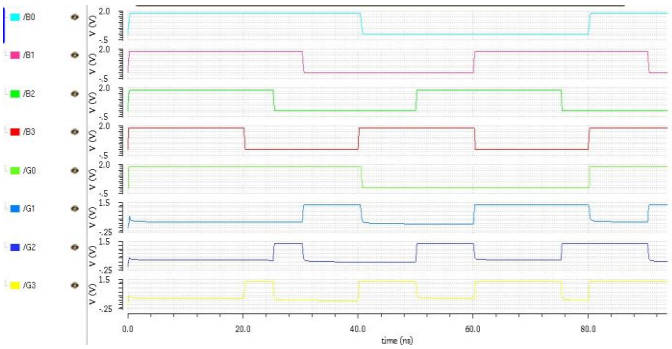


Fig.20. Transient response of Binary to Gray Code Converter implemented using Toffoli gate with PTL-based XOR.

The transient waveform as shown in Fig.20 verifies proper operation of the converter and shows improved performance in terms of power efficiency compared to the non-PTL Toffoli implementation.

C. Binary to Gray Code Converter Using Feynman Gate with PTL based XOR

The Feynman gate is a 2×2 reversible gate whose functionality depends on XOR operations. By replacing the conventional XOR with a PTL XOR, the overall transistor count of the Feynman gate and consequently the converter is significantly reduced. This PTL-based Feynman gate retains reversibility while improving energy efficiency.

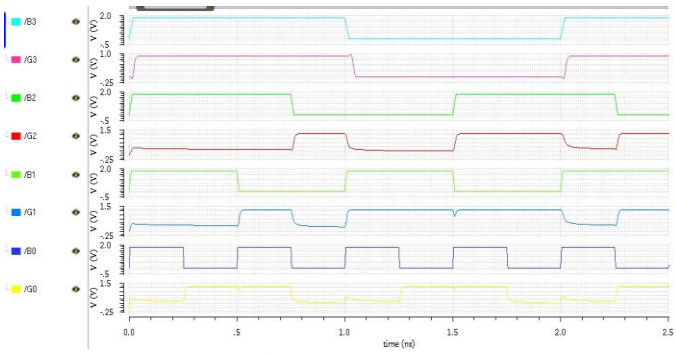


Fig.21. Transient response of a Binary-to-Gray code converter implemented using Feynman gates with PTL-based XOR

The transient response Fig.21 shows correct gray code generation with lower power dissipation. This implementation achieves the **b**est power efficiency among all the tested designs, reducing power consumption by up to 90.15% compared to the conventional XOR-based converter.

X. Results and Discussion

Various XOR gate implementations were designed for a 4-bit Binary to Gray Code converter and analyzed for their performance in terms of power consumption, delay, and transistor count, as summarized in Table IV. The conventional XOR gate consumes 32.98 µW of power, with a delay of 12.65 ps and 40 transistors, serves as the baseline for comparison.

The XOR gate implemented with Transmission Gate Logic architecture illustrates better power efficiency, consuming 31.30 µW, which corresponds to a 5.09% reduction in power consumption with respect to the traditional design. This implementation maintains a similar delay of 12.65 ps while reducing the transistor count by about 30%, offering a more compact and balanced solution in terms of power, speed, and layout simplicity.Reversible logic gates such as the Toffoli and Feynman gates offer significant improvements in energy efficiency, albeit with increased circuit complexity. The Toffoli gate has a power consumption of 4.937 µW, providing an 84.91% reduction over the conventional XOR gate. It uses 82 transistors with a delay slightly higher at 39.51 ps, thus providing excellent power saving without significant degradation in timing.The Feynman gate results in the least power dissipation among all the conventional reversible designs, with a power of only 3.247 µW, representing a 90.15% power reduction compared to the conventional XOR implementation. However, this improvement in energy efficiency is made at the expense of higher delay, 39.11 ps, and increased transistor count, limiting the suitability of this approach for high-speed applications or area-limited designs.Further, power optimization was achieved when the designs based on PTL were considered. The Feynman gate with the XOR implemented using PTL logic showed outstanding power efficiency, saving about 98.7% power compared to the conventional XOR gate while improving the

delay by about 14% and bringing down the transistor count to 25. Similarly, the conventional XOR implemented in PTL logic required 141.8 µW of power with a delay of 12.67 ps and 12 transistors, showing outstanding power-delay-area characteristics. However, the Toffoli gate implemented using the PTL logic showed a higher power dissipation of 14.53 mW, probably due to greater switching activity and internal node loading during its operation. Although with a heightened power consumption, Toffoli gate was functionally correct and gave insight into the trade-offs involved with the integration of PTLs and reversible gate complexity.

TABLE IV
COMPARISON TABLE FOR PROPOSED METHODOLOGIES

S.No.	Binary to Gray code convertor using	Parameters			
		Power	***Delay***	***Number of transistors***	
1.	Conventional XOR gates in 180nm	20.24 **µW**	56.8 ps	48	[12]
2.	Conventional XOR gates in 90nm	32.98 **µW**	12.65 ps	40	
3.	Conventional XOR gates using PTL logic	141.8 **µW**	12.67 ps	12	
4.	Transmission Logic	31.30 **µW**	12.65 ps	28	Proposed work
5.	Toffoli Gate	4.937 **µW**	39.51 ps	82	
6.	Toffoli Gate using PTL logic	14.53 mW	2.184 ns	61	
7.	Feynman Gate	3.247 **µW**	39.11 ps	52	
8.	Feynman Gate using PTL logic	421.2 nW	10.90 ps	25	

XI. CONCLUSION

A highly efficient approach for the conversion of 4-bit Binary to Gray code was developed using a variety of design methodologies, such as conventional, transmission gate, and Pass Transistor Logic (PTL) implementations of XOR gates, and some reversible logic gates like Feynman and Toffoli gates. All the designs are implemented and simulated on Cadence 90 nm CMOS technology for their power, delay, and transistor count.Among all the designs, the Feynman gate implemented using the PTL-based XOR has the lowest power dissipation, which is around 98.7% less as compared with a conventional XOR-based converter, with an approximately 14% improvement in delay. The Toffoli gate exhibited an 85% reduction in power, relative to the conventional XOR design, although with higher delay and transistor usage. Meanwhile, the transmission gate-based converter has a modest 5% reduction in power dissipation, with negligible variation in terms of delay, using a 30% lower number of transistors.

In contrast, the PTL-based XOR Toffoli gate showed a much higher power consumption, probably because of greater switching activity and internal loading during simulation, although it also provided the right functional behavior. However, both Feynman- and Toffoli-based designs demonstrated the potential of reversible logic in reducing energy dissipation by preserving information during computation.

The Feynman gate with PTL-based XOR outperformed all other implementations in terms of both power and area, while the Toffoli gate provided a reasonable trade-off between design complexity and performance. These results confirm that the application of PTL principles to the field of reversible computing logic allows for a significant reduction in energy dissipation within VLSI circuit designs, thus making them highly appropriate for IoT, embedded, and portable electronic applications that require minimum power consumption.

ACKNOWLEDGEMENT

The authors would like to thank the organization and Meity C2S Project for providing necessary tools, Chaitanya Bharathi Institute of Technology (A), Affiliated to Osmania University, Hyderabad for the support provided for carrying out this work.

Competing Interests: The authors have no conflicts of interest to declare that are relevant to the content of this chapter.

REFERENCES

[1] N. Varshini and V. Siddeshwara Prasad, "Design and Analysis of Binary into Gray code converter using Cadence 180nm Technology," 2024 First International Conference on Innovations in Communications, Electrical and Computer Engineering (ICICEC), 2024, https://doi.org/10.1109/ICICEC62498.2024.10808533

[2] Sharmila Devi Shanmugam, "Enhanced Low-Power DSP via a Novel Reversible MCML-Based Carry-Select Adder," *Trait Signal*, Apr. 2024, https://doi.org/10.18280/ts.410245

[3] Neeraja Bandi, Rajkumar Ramavath, and Sathish Kumar Meda(2020) Design and analysis of PTL based basic gates and adder with improved performance in Proc. Int. Conf. Recent Trends Electron., Inf., Commun. Technology(RTEICT),pp.184-188. https://doi.org /10.1109/RTEICT49044.2020.9315581

[4] Morrison, Matthew, Matthew Lewandowski, Richard Meana and N. Ranganathan. "Design of static and dynamic RAM arrays using a novel reversible logic gate and decoder." *2011 11th IEEE International Conference on Nanotechnology* (2011): 417-420. https://doi.org/10.1109/NANO.2011.6144407

[5] T. Hirayama et al., "An Improved lower bound on the gate count of Toffoli-based reversible logic circuits", IEICE Trans. Inf. & Syst., vol. E97-D, no. 9, pp. 2253–2261, 2014. https://doi.org/10.1109/ISMVL60454.2024.00032

[6] Thapliyal, Himanshu and N. Ranganathan. "Design of reversible sequential circuits optimizing quantum cost, delay, and garbage outputs." 2010 23rd International Conference on VLSI Design pp 235-240. https://doi.org/10.1109/VLSI.Design.2010.74

[7] Tian Y., Liu Z., Ying T., Xiao H., Meng Y., Deng L., Zhao Y., Guo A., Liao M., Liu G., Yang J., "Experimental demonstration of an optical Feynman gate for reversible logic operation using silicon micro-ring resonators", *Nanophotonics*, vol. 6, no. 5, pp. 847-852, 2017. https://doi.org/10.1515/nanoph-2017-0071

[8] K. Batish, S. Pathak, and R. Gupta, "Comparative Analysis for Performance Evaluation of Full Adders Using Reversible Logic Gates,"

2018 International Conference on Intelligent Circuits and Systems (ICICS), 2018, pp. 126–132, https://doi.org10.1109/ICICS.2018.00036

[9] S. Parvin and M. Altun, "Implementation of CMOS Logic Circuits with Perfect Fault Detection Using Preservative Reversible Gates" 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS), 2019, pp. 64–67, https://doi.org/10.1109/IOLTS.2019.8854440

[10] Khakpour, Mahdi, M. Gholami and Shokoufeh Naghizadeh. "Parity generator and digital code converter in QCA nanotechnology." *International Nano Letters* 10 (2019): 49-59.

[11] P. Tomar, P. P. Bansod, R. C. Gurjar, and R. Jarwal, "Realization of testable D Flip-Flop based on reversible logic," 2021 5th International Conference on Information Systems and Computer Networks (ISCON), 2021, pp. 1–6, https://doi.org/10.1109/ISCON52037.2021.9702499

[12] T. Sangeetha, S. Sahithya, P. Mouliga, S. Padmapriya, M. Jagadeeswari, and V. Anbumani, "Design of Reconfigurable Reversible Low Power Adders" 2023 Third International Conference on Artificial Intelligence and Smart Energy (ICAIS), 2023, pp. 175–179, https://doi.org/10.1109/ICAIS56108.2023.10073896

[13] Bari, Surajit, Debashis De and Angsuman Sarkar. "Design of low power, high speed 4 bit binary to Gray converter with 8 × 4 barrel shifter using nano dimensional MOS transistor for arithmetical, logical and telecommunication circuit and system application." *Microsystem Technologies* 25 (2017): 1585 - 1591. https://doi.org/10.1007/s00542-017-3435-4

[14] M. Haghparast and K. Navi, "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems," *Journal of Applied Sciences*, vol. 7, no. 24, pp. 3995–4000, Dec. 2007. https://doi.org/10.3923/jas.2007.3995.4000

[15] S. S. Chiwande and P. K. Dakhole**,** "Ultra Efficient Reversible Logic Multiplier Design and Implementation for Low Power Application" *International Journal of Intelligent Systems and Applications in Engineering*, vol. 12, no. 10s, pp. 415–422, Jan. 2024.Retreived from https://ijisae.org/index.php/IJISAE/article/view/4390

[16] Landauer, R., 1961. Irreversibility and heat generation in the computing process, IBM J.Research and Development, 5 (3): 183-191. https://doi.org/10.1147/rd.53.0183