

Design Considerations for High-Speed Read-Out Integrated Circuits for Photonic Integrated Circuits

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Abstract—Photonic integrated circuits often need a dedicated electronic device to communicate with the external world. Often a dedicated Read-Out Integrated Circuit is preferred. In this work the design considerations for high-speed ROICs are presented. A set of key specifications is discussed. Then, selected ROIC chip-level topics are presented. Finally, the issues related to the experimental testing and system-level development are considered.

Keywords—PIC; ROIC; TIA; ASIC

I. INTRODUCTION

PHOTONIC integrated circuits (PICs) are an extremely important topic in optoelectronics [1]. Although near-infrared (NIR) PICs are heavily developed due to the demand in data- and telecommunications, there is a huge work to be done to develop PIC technologies for other bands (e.g. mid- and far infrared). The most common applications for PICs are: data and telecommunications, medical diagnostics and automotive.

Photonic systems can have many various components, playing different roles in the application. The most important ones are:

- light source (lasers, LEDs);
- photonic passives – devices that process optical signal without external factor (power or modulation signal): e.g. waveguides, couplers, multiplexers;
- photonic active devices – directly processing the optical signal with external factor: amplifiers, modulators, etc.;
- photonic detectors (photodiodes (PDs), photoresistors, phototransistors) that convert the light signal to the electrical domain (like current, resistance or voltage).

The photonic components are often made in different manufacturing processes, created in different materials, making the system integration even harder.

To effectively capture the electrical signal at the output of the photodetectors, often Read-Out Integrated Circuits (ROIC) are needed. ROICs convert the signal generated by the photodetector (e.g. current) to voltage and provide an interface between the photodetector (mainly photodiodes) and the external world. Without ROIC, a PIC-based system can have limited performance. ROIC allows the signal to be read using standard measurement or data acquisition equipment (oscilloscopes, spectrum analyzers or analog-to-digital converters (ADCs)).

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In this paper the design considerations for the ROICs operating in high-frequency regime (>100 MHz 3dB bandwidth) are presented. This paper focuses on achieving optimum solution for given constraints. It can be also useful for PIC engineers to better understand the limitations that comes with ROIC, as well as better specify the constraints for ROIC parameters.

II. ROIC SPECIFICATIONS

ROIC specifications are derived from the role defined by the system. First of all, the input side should be considered. The following issues have to be taken into account:

- Detector's electrical parameters: dark current I_d , saturation current I_s , equivalent capacitance C_{pd} , parallel resistance R_p , and series resistance R_s . Fig. 1 presents the basic photodiode model that should be discussed before the ROIC design.

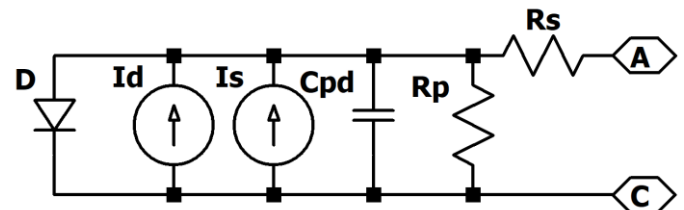


Fig. 1. Basic photodiode model, it may be enhanced with other parameters, e.g. lead inductances.

- Input signal parameters (current range, bandwidth, slope).

Secondly, the output side should be considered, specifically:

- Type of device connected to the output of the ROIC.
- Expected output capacitance, impedance, etc.
- Connection type (bond wire, PCB traces).

Last, but not least, the internal ROIC parameters should be discussed:

- Supply voltage and power consumption.
- Dimensions of the chip.
- Number of pins/pads.
- Conversion type (binary On-Off Keying (OOK) signal or linear).

In this paper, we focus more on ROICs with linear conversion. However, it's still worth mentioning because one

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can find many high speed OOK amplifiers for telecommunications, which cannot be easily adopted to linear applications.

The aspects covered in this section should be considered in great detail before designing a high-speed PIC system with ROIC on board, because these effects can severely limit the overall performance of the system. Every component should be included in the calculations and simulation.

III. CHIP-LEVEL CONSIDERATIONS

Once the specifications for the ROIC (goals and constraints given by the PIC system) are collected, IC designers can start to consider chip-related issues:

- Manufacturing process node.
- Internal functional structure (schematic).
- Functionalities and features (gain control, filtering, testability).
- IC layout issues.

A. Manufacturing process considerations

The specifications of the ROIC manufacturing process are driven by a couple of factors. The most obvious are cost and access to the IC manufacturing process. Both the prototyping cost and scaled-up volume production cost should be considered. Also, the prototyping and production schedule (a.k.a. *runs*) may be a factor when deciding on the specific IC fabrication process.

Bipolar ICs have lower noise [1]. MOSFET-based devices (like CMOS) have significant flicker ($1/f$, pink) noise. However, CMOS processes are more common, more affordable and can achieve higher level of integration with other circuits (e.g. digital electronics). There are also hybrid technologies, such as BiCMOS or BCD available in the market; however, they are not so popular, therefore the production schedules and costs are not so suitable.

There are also differences between manufacturers in a similar process. Devices fabricated in e.g. 180 nm bulk CMOS from various foundries have different cut-off frequencies and different noise performance. Before choosing a specific process node, a broad, yet detailed analysis of available nodes would be helpful. In this paper we will focus on CMOS circuits due to the wider availability of CMOS process nodes.

B. Internal functional structure

1) Input amplification – transimpedance amplifier

Input stage plays a critical role in the whole ROIC. This role is to amplify often weak signals with low noise. The most common input stage for linear conversion from the photodiodes is a transimpedance amplifier (TIA). This circuit converts the current signal from the photodiode to the voltage signal that can be easily read by the measurement or acquisition equipment. The most common realization is a topology with operational amplifier OA and the resistor R_f in the feedback loop (Fig. 2). C_f capacitance is used to ensure the stability of this feedback circuitry. The -3 dB bandwidth of transimpedance gain can be approximated by the following formula (A is gain-bandwidth product of OA, C_{in} is overall capacitance seen at the input):

$$f_{-3dB} = \frac{A}{2\pi R_f C_{in}}$$

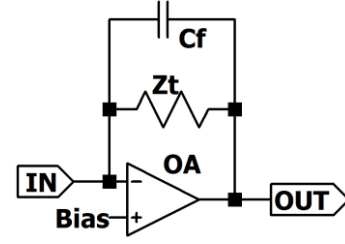


Fig. 2. Basic transimpedance amplifier (TIA) circuit, based on operational amplifier.

When high-speed operation is needed, one should consider the limitation of transistors in the input transimpedance amplifier. Unity-gain stable amplifiers are not the best choice for amplifying component because decompensated amplifiers offer better noise and bandwidth specifications [2]. Fig. 3 shows a simplified schematic of TIA with a few transistors.

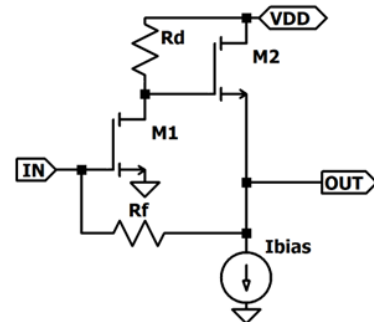


Fig. 3. Transimpedance amplifier with common source input stage, common drain output buffer and feedback resistor.

Please note that the circuit in Fig. 3 is not immune to the large output load or changes in output load. This change can affect the bandwidth or stability of the feedback loop. It is recommended to isolate the output from the feedback system [3]. To do that, another amplifier stage should be added, similarly to Fig. 4.

Although diodes provide single-ended current signal, differential readout circuits can be employed. Consider the solution in Fig. 5. The input current signal is fed to common gate input stage. Then the converted signal is directed to differential pair (M2, M3), which not only amplifies the signal, but additionally converts the single-ended signal to differential one. Hence, the improved supply noise rejection can be achieved.

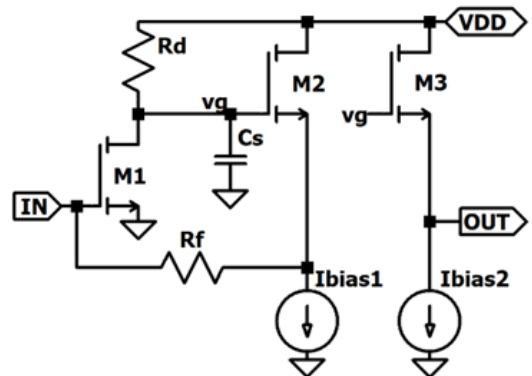


Fig. 4. TIA with feedback loop separated from the output.

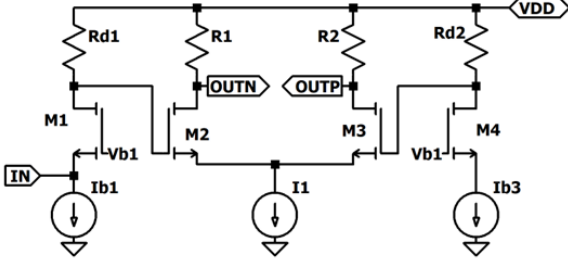


Fig. 5. TIA with common-gate input, output differential pair, and common gate stage (M4) for improved symmetry.

With the design of TIA comes specific *gain-speed-noise tradeoff*. As studies show, to reduce the total integrated noise, it is needed to increase the transimpedance gain by increasing the resistance in the feedback [4]. However, this limits the bandwidth of the amplifier [3]. The designer should discuss design goals and constraints, since these parameters need optimization.

To achieve high-speed operation of input TIA, the following should be considered:

1. The gain should be relatively small: the transimpedance of megaohms can severely limit the bandwidth. On the other hand, the input-referred current noise i_{eqi}^2 which is inversely proportional to resistance setting the transimpedance gain, should be considered:

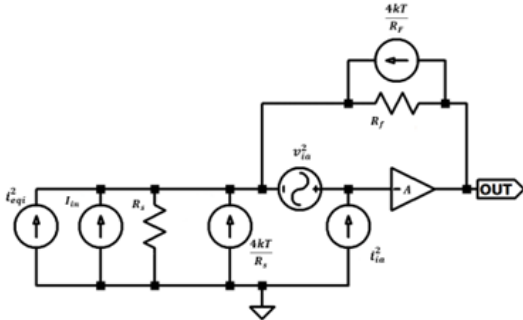


Fig. 6. Transimpedance amplifier with different noise sources explained.

$$i_{eqi}^2 = \frac{4kT}{R_s} + \frac{4kT}{R_f} + i_{ia}^2 + \frac{v_{ia}^2}{(R_s || R_f)^2} + 2\Re\left(\frac{i_{ia}^* v_{ia}}{R_s || R_f}\right) [4],$$

Where:

i_{ia} : amplifier's internal input-referred current noise,
 v_{ia} : amplifier's internal input-referred voltage noise,
 R_s : photodiode series resistance,
 R_f : feedback loop resistance,

2. The feedback loop should be as simple as possible: any addition of switches or other devices (e.g. to realize gain control) can add the undesirable capacitance that reduces the bandwidth;
3. Optimum bias conditions for input transistor/diff pair should be found for maximum unity-gain bandwidth [5] [6].

2) Output stage – line driver

When transmitting high-speed ($f > 100$ MHz) signal through the systems, the output stage should be designed carefully. Directly connecting the oscilloscope or even high-speed oscilloscope probe (with 1 pF of input capacitance) to unbuffered TIA may limit the performance of the ROIC. This is why the output buffer stage should be designed.

The output driver design is constrained by the signal characteristics expected from the TIA and by the expected load. Good linearity is expected, therefore class A or AB buffers should be considered. In Fig. 7 a good CMOS AB line driver is presented [7]. This circuit, when properly designed, can achieve rail-to-rail operation.

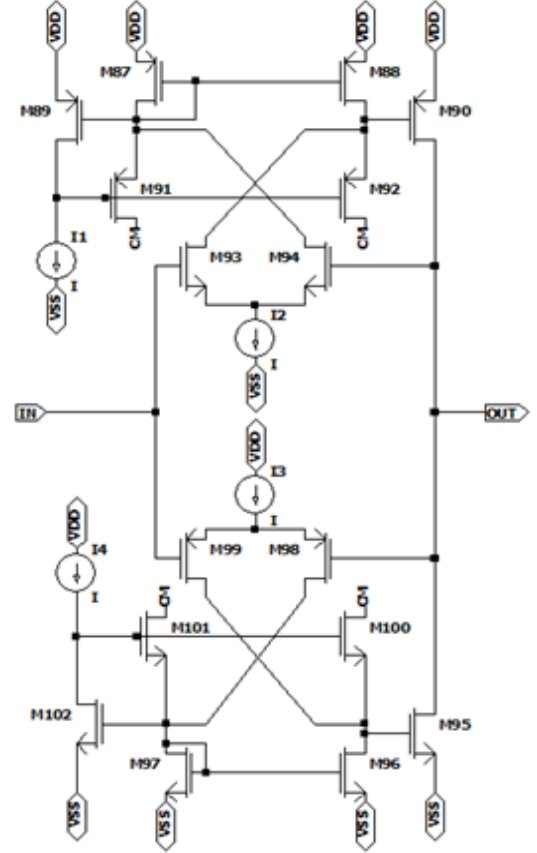


Fig. 7. CMOS AB output buffer with possibility of rail-to-rail operation [7].

For even better integration scale, the use of on-chip analog-to-digital converter (ADC) may be considered. This can help to limit the influence of the noise. However, this can drive up the cost of ROIC design and manufacturing really high.

C. Auxiliary circuitry and features

Both input and output stages should be biased properly. For transimpedance amplifiers based on operational amplifiers a stable voltage bias for the positive input pin may be needed. This can be achieved by the usage of bandgap reference (BGR) based voltage references, immune to temperature changes and supply noise.

For diagnostics purposes some test points can be added. However, the impact of diagnostics ports should be considered carefully. Any additional connection to the signal path, especially when considering feedback loop, can have tremendous impact on bandwidth. This issue also applies to the gain control feature, which is typically realized by the parallel resistors and switches (transmission gates).

Often it is desirable to remove the DC component of the signal (e.g. when the device is working in environment with daylight access). This function is commonly referred as ambient light cancellation (ALC) [8] or DC cancellation [9]. This is often realized by the current sources that add or subtract DC current from the input (Fig. 8).

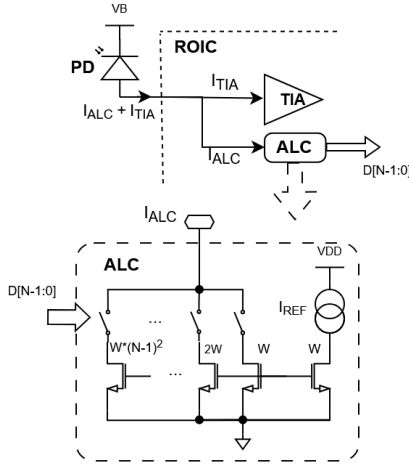


Fig. 8. ROIC with ALC block (top) and typical digitally-controlled ALC (binary-weighted current mirror, bottom)

D. IC layout considerations

For layout design, apart from the typical analog layout design principles (e.g. matching), there are couple of issues that should be considered (depicted in Fig. 9):

- Use low-capacitance bonding pads and I/O structures (while maintaining required ESD protection level).
- Keep input amplifier structure close to the pad (keep short input track) to reduce parasitics at the input.
- Keep dummy structures away from input path to reduce undesirable capacitance (maintain the minimum layers density for DRC compliance).

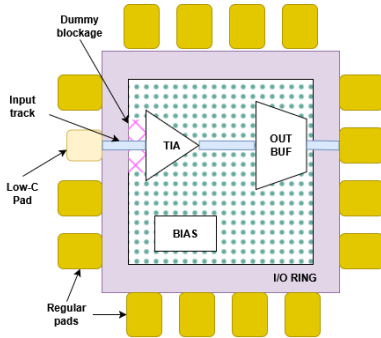


Fig. 9. Layout considerations for high-speed linear ROIC inputs

IV. SYSTEM-LEVEL CONSIDERATIONS

In this section emphasis will be placed on experimental tests and application environment. Badly realized environment and test procedure may affect the outcomes. In this section chosen aspects of testing and application will be discussed.

A. Input capacitance

Capacitance at the input C_{ieq} (combined: photodiode capacitance C_{pd} , interconnection capacitances $C_{PCB,a}$ and $C_{PCB,b}$ and ROIC input stage capacitance $C_{ROIC,IN}$) leads to the one of the most limiting factor for the bandwidth of the PD-ROIC system. Please consider case in Fig. 10. The C_{ieq} together with the feedback resistance R_f of the ROIC create the low-pass filter. This can lead to reduction of the bandwidth of the PIC system.

There are number of techniques that may reduce the capacitance seen from the input of the ROIC:

- Photodiode intrinsic capacitance C_{PD} : This can be reduced by the reverse polarization. However, consider the voltage levels at the input of the ROIC (to maintain SOA of the input transistors);
- Keep bond wires and traces possibly short. This reduces not only the capacitance but also inductance. Flip chip and stack techniques with solder bumping are preferred;
- Keep ground fill away from the signal path on PCB/RDL (redistribution layer). This reduces parasitic capacitance between signal path and ground plane. This applies to all the layers in the PCB/RDL stack.

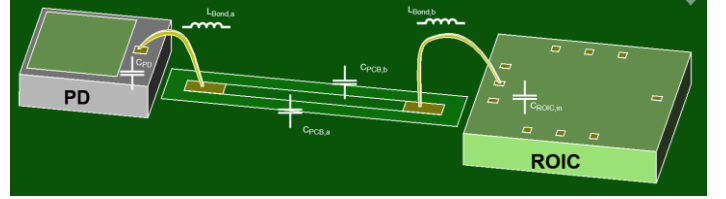


Fig. 10. Model explaining different parasitic elements between photodiode and ROIC.

B. Simulating the photodiode in experimental tests

Before the testing of the PD+ROIC system, the electronics designer may want to test only the ROIC performance. To do it, it is essential to create an imitation of signal expected from the photodiode. Since high-speed current signal generator may not be available, the easiest way is to put the resistor between the output of the voltage signal generator and ROIC analog input.

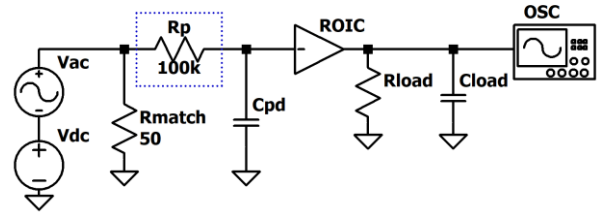


Fig. 11. ROIC Test circuit idea, with voltage signal generator and resistor in series at the input. Based on [8].

C. Input-output and diagnostics interconnects

The most common way of delivering a high-speed signal to measurement equipment is use of coaxial cables. This transmission lines provide shielding from the external noise. Measurement equipment, e.g. oscilloscopes, signal analyzers or vector network analyzers (VNAs) often have N, BNC, SMA or another coaxial connector at the input.

When designing the test environment, special attention should be paid to the cable assemblies (namely connectors (Fig. 12)) and cables (Fig. 13)). Different connectors represent different parasitics. It is recommended to use the smallest ones such as U.FI or MCX. It is also advised to limit the number of any adapters (like BNC to SMA adapters) because they may affect the signal path.

There are several aspects that should be considered before designing or selecting ROIC for a given application:

- Type of device connected to the ROIC's output. The type of input that ROIC represents.

- Type of connector (SMA, BNC, N, MMCX) and transmission line (RG-59, RG-174, RG-316), together with connection length.
- ROIC connection method (via bond wire or solder bump). Connection to the package or directly to the substrate.



Fig. 12. Various types of coaxial connectors.



Fig. 13. Various types of coaxial transmission lines.

D. Input-output and diagnostics interconnects

For high speed operation of the ROIC, the inputs are expected to be at certain DC level (operating point). On the other hand, the photodiodes represent lower capacitance when reversly-biased. Once directly connected, the bias of the PD can affect ROIC parameters. Also, high bias (couple of volts) can be destructive for ROICs manufactured in advanced, low-voltage processes. Therefore, the DC separation should be considered (Fig. 14). This leads to 2 obvious disadvantages: First, the placement of another component in the device. Unfortunately, IC on-chip capacitances (MIM, MOM) have small unit capacitance and can have significant parasitics (equivalent series resistance and substrate capacitance) for high speed

operation. Consequently, a rather small chip capacitor, e.g. 0201, should be considered. Second, there will be high-pass filtering in the system (DC and low frequency signals will not be propagated through the system). The designers should consider the maximum capacitance available in the smallest case, with a good dielectric (COG, NPO or X7R).

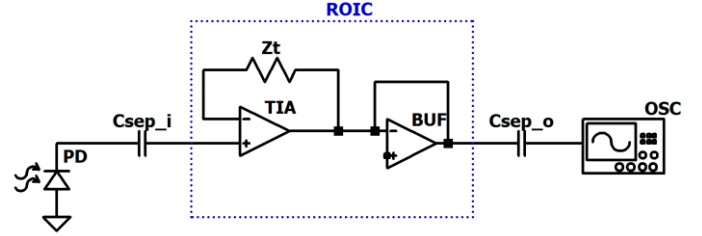


Fig. 14. DC separation idea: C_{sep_i} capacitance at the input and C_{sep_o} at the output.

CONCLUSION

In this work, the design and test considerations for high-speed ROICs for photonic integrated circuits were presented. A basic specification list is highlighted, several chip-level solutions are shown, and a couple of system-level issues are discussed. This paper is meant to be a common starting point for PIC with ROIC system design.

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