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Switched Current Sigma-Delta Modulator with a New Comparator Structure Designed Based on VHDL-AMS Description

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***Abstract*—The paper presents a VHDL-AMS based approach to the Switched-Current (SI) Sigma-Delta Modulator design. The prototype VHDL-AMS description, with the help of elaborated EDA tools, is automatically translated into the SI realization. Another tool helps the designer to create the layout. The paper also describes a new current mode comparator, which is used in the design. Postlayout simulation results are presented.**

***Keywords*—Switched-Current, VHDL-AMS, sigma-delta modulator**

I. Introduction

THE development of new electronic technologies leads to increasing the complexity of modern System on Chip devices (SoC). They contain the whole analog and digital processing chain. Even though many algorithms realized earlier in analog systems have already been implemented in digital, there are still circuits which can be realized only in the analog domain. An obvious example is an analog-to-digital converter. New technologies, which have achieved nanometers dimensions, cause new challenges both at the stage of the design stage and the production stage of integrated circuits. New technologies offer faster transistors, but introduce new nonidealities, which cause the smaller accuracy of elements.

To minimize problems with low accuracy of elements for A/D converter design, sigma-delta structure is a good approach. SD structure does not require accurate elements, offering the expected speed and resolution. Switched capacitors (SC) and switched currents (SI) are common techniques used for SD converters realizations. However, one of the advantages of modern nanotechnology, reduction of the supply voltage, causes new problems for SC technique such as the signal swing reduction and reduced transconductance of the switches. This opens new possibilities for SI, which can find applications in the systems, where small power consumption is essential but high resolution of the processing is not a necessity.

State of the art sigma-delta modulators are presented in [1] and prospective SI circuits are discussed in [2]. These publications show that the topic is still important and further development is required. It is also a motivation to work on further improvements of the existing SI elements. Moreover, it justifies the development of EDA tools, which help designers to minimize time to market for the analog part of the System on Chip devices.

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This paper presents EDA tools elaborated for the SI class of circuits. Practical verification of the proposed approach is illustrated with the design process of the switched current Sigma-Delta Modulator (SDM). The VHDL-AMS language is used in the tools to describe the designed circuit. This approach is continuation of works presented in [3].

The paper is organized as follows. Section II is a review of main SI blocks elaborated by authors, including new proposed current comparator. Section III presents the design flow used in the proposed approach and describes the EDA tools elaborated to automate the SDM design process. Section IV shows the layout of the prototype chip and postlayout simulation results. Finally, the last section summarizes the achieved results.

II. Basic Components

The proposed SI Sigma Delta Modulator is composed of blocks elaborated by authors [4], [5]. This section provides a short review of these blocks, but mainly focuses on new proposed blocks, i.e. the DC-offset compensation block and current comparator.

A. Memory Cell

Several basic memory cells have been presented in the literature. The simplest memory cell is based on a current mirror which has a switch added between the transistors [6]. The parasitic gate capacitance stores the voltage and the current mirror generates the output current. To cancel the mismatch effects of transistors used in the current mirror, the second generation memory cell has been introduced [7]. This structure is based on one transistor and three switches. Due to using two non-overlapping clocks the same transistor is used in two phases: in the first phase, voltage corresponding to the input current is stored; in the second phase output current is produced. In order to minimize parasitic effects in the second generation memory cell, various memory cell structures have been developed. A balanced structure is used in order to cancel DC offset and clock feed-through error; a grounded-gate feedback structure is used for minimizing transmission error in cascaded memory cells. The SI blocks used in our approach are based on the memory cell proposed by the authors and verified in practical realizations [8]. This basic cell has been

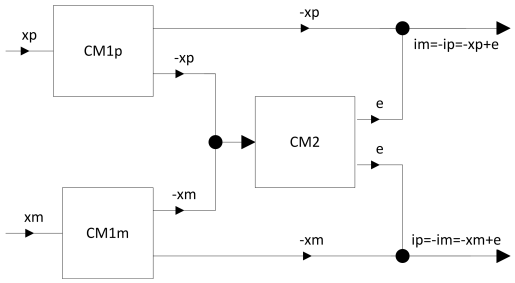

Fig. 1. Compensation block structure.

used to compose more complex blocks, which are necessary in SDM implementation.

B. Compensation Block

A fully differential approach makes possible compensation of the parasitic effects in balanced structure circuits: the DC offset, the clock feed-through, the charge injection effects and the harmonic distortion. This approach also improves CMRR. The compensation block structure is presented in Fig. 1. This block makes simple arithmetic operations on noisy current inputs xp and xm to get desired clean outputs ip and im [9]. The input currents have an additional, undesired DC-offset denoted as e. The relation between input and output signals can be written as follows

$$xp[n] = ip[n] + e, \quad xm[n] = im[n] + e \tag{1}$$

The balanced structure implies the relation $ip[n] = -im[n]$, hence the error to be canceled can be worked out from Equation 1 and is equal to

$$e = (xp[n] + xm[n]) : 2 \tag{2}$$

Now, we can simply subtract it from the input signal, as shown in Equation 3.

$$ip[n] = xp[n] - e, \quad im[n] = xm[n] - e \tag{3}$$

The described operations are implemented by current mirrors with the adequate number of outputs and scaling factor values. According to the notation used in Fig. 1, the first two blocks $CM1p$ and $CM1m$, are current mirrors with two outputs, which provide two copies of the input currents (scaling factor 1.0) needed for further processing. One of them is used to calculate the error e, and the other is used to perform the final subtraction. Two output current mirror CM2 provides half of its input current (scaling factor 0.5) in both outputs. The proper sign of the signals needed to perform the subtraction is obtained thanks to the different number of current mirrors in each path. The described compensation circuit was used in the design circuit and will be recalled in next subsections.

C. Integrator

The main block of any SDM structure is the noise shaping filter. This function is realized by an integrator. The proposed SDM uses a bilinear, fully differential integrator, proposed by authors and described in detail in [4]. In this paper we propose a modification of this integrator, which consists in adding the compensation blocks (see Fig. 1). These blocks were included in the input path of the integrator to cancel the DC-offset from the previous stages and to protect the integrator from achieving saturation. The integrator is treated as a library component for a given technology. In our design flow the integrator has different views: the prototype VHDL-AMS entity with behavioral architectures, the SI VHDL-AMS entity, the SPICE description at the transistor level and finally the layout. Of course the transistor level and layout views are technology dependent. The proposed structure of the integrator was fabricated in AMS $0.35\mu m$ and after the transistor sizes recalculation in TSMC $0.18\mu m$ as well. Measurement results of both realizations have proved the correctness of the proposed solution. Detailed results are presented in [8].

D. Comparator and D/A Converter

This paper presents a new approach to comparator and D/A converter implementation, which is used in the prototype SDM structure. A novel idea consists in combining both components into a one functional block, and designing it in fully differential current mode. The first designs of SI SDM use a simple inverter as a current comparator [10]. However, in current mode circuits, such inverter is usually loaded by diode connected transistors. This means that the typical load has a low input impedance. Additionally, high resistance input of the inverter lengthens the integrating time of current excitation. The response time can be shortened if a complementary pair of MOS transistors are added on the input of the inverter to decrease the resistance of this input. This additional transistor pair can be diode-connected, which forms a current-to-voltage converter. Another solution was proposed by Träff [11], where the nMOS transistor changes place with the pMOS transistor in comparison to an inverter. One more solution for high speed, high dynamic range current comparator was presented by Banks and Toumazou [12]. This circuit is composed of three inverters and a diode connected transistor pair in each positive and negative path.

Our proposal of a new current mode comparator structure is presented in Fig. 2. The circuit is divided into two blocks. The input stage is based on the Schmitt trigger or on the Träff structure. The output block is an OTA amplifier with a preamplifier stage to improve the dynamic range of the signal [13]. OTA output stage is a differential amplifier, which gives the required output currents. The current amplitude can be regulated with appropriately chosen bias voltage. The difference between the Träff based and Schmitt based solutions consists in different power consumption and in different response time. The Träff based structure consists of two typical Träff comparators for both inputs. The circuit based on Schmitt trigger, presented in Fig. 3 has diode connected transistor pairs (M3M4 and M9M10) on its inputs. It converts input current into voltage, which is further applied to a standard inverter based comparator (M1M2 and M7M8). We propose to add a Schmitt trigger which improves the sensitivity of the comparator. The balanced structure of the comparator allows

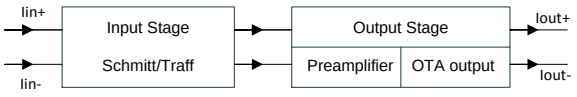

Fig. 2. Current comparator structure.

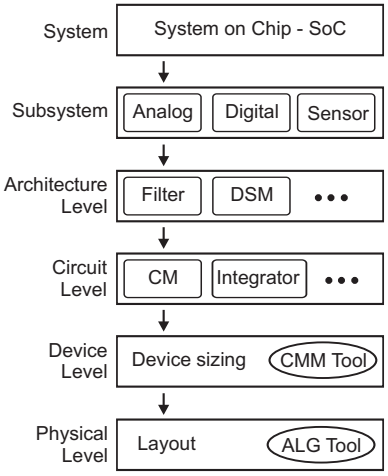

Fig. 4. Design flow of SI circuits.

us to use only one Schmitt trigger connected to both (inverting and noninverting) inputs of the comparator. Using the Schmitt trigger we can realize a faster but more power consuming current mode comparator. Current outputs of the comparator allow us to connect this block directly in the feedback of a current mode SDM.

The input stage can be composed of the Träff comparator instead of the Schmitt trigger. The difference between both solutions consists in different power consumption and response time. We observe the response delay dependence on the current swing on the input of the comparator. The smaller the input signal, the longer the response delay. The comparator composed of the Schmitt trigger is faster than the one composed of the Träff cell at the expense of power consumption.

III. Design Flow

This section presents the design automation process. Referring to the Fig. 4, the proposed design flow includes the design of the architecture, circuit, device and layout levels. It starts from the SD structure chosen by the designer and finishes with the layout of the complete SI circuit automatically generated for a given technology. In this section we will focus on the translation between the architecture and circuit level.

A. VHDL-AMS Description

VHDL-AMS was chosen as a language to describe the design. It allows us to simulate mixed, analog-digital design and assures the consistency throughout all the steps when designing complex integrated systems such as microsystems including sensors and actuators. Additionally, it makes the design independent of specific graphic entry tools.

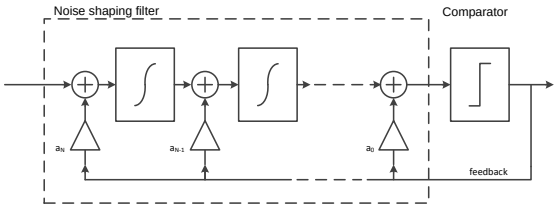

Fig. 5. A general feedback type structure of Sigma-Delta modulator.

At the beginning of the process, the designer can use several basic entities to build a desired SDM structure. Every SDM consists of a noise shaping filter, comparator, scaling elements and summation blocks. Figure 5 shows a general structure of a feedback-type SDM. Other possible types are feed-forward and MASH, which also can be built with the same blocks. Depending on the filter order, the SDM is the first, second, third etc. order. In practical realization higher order modulators are not implemented because of the stability problem. The noise shaping filter includes the integrators, summing elements and, if it is required, the scaling blocks.

For the purpose of design the structural VHDL-AMS is used. However, the architecture of each basic component can be included at any time and used to verify the project in different levels of abstraction. As an example the VHDL-AMS description of the first order SD prototype structure is presented below.

```
    -- Sigma-Delta 1st order
library ieee;
use ieee.std_logic_1164.all;
use work.all;

entity SD_1ORDER_OK is
end entity SD_1ORDER_OK;

architecture arch_SD_1ORDER_OK of SD_1ORDER_OK is
   signal O_DAC: REAL;
   signal OUT_SD1: STD_LOGIC;
   signal IN_SD1: REAL;
   signal O_INT: REAL;
   signal O_LIN: REAL;
begin
   INT1 : entity WORK.SD_INTEGRATOR(IDEAL)
      port map ( INPUT => O_LIN, CLK => OPEN, OUTPUT => O_INT );
   LIN_COM1 : entity WORK.SD_LINCOMB(IDEAL)
      port map ( INA => IN_SD1, INB => O_DAC, OY => O_LIN );
   COMP1 : entity WORK.SD_COMPARATOR(IDEAL)
      port map ( INPUT => O_INT, OUTPUT => OUT_SD1 );
   DAC1 : entity WORK.SD_DAC1B(IDEAL)
      port map ( INPUT => OUT_SD1, OUTPUT => O_DAC );
end architecture arch_SD_1ORDER_OK;
```

This VHDL-AMS text file is a starting point of the design flow. For further reference let us name it as a prototype SD structure. At this stage, behavioral architectures of the circuit can be used for simulation. Different architectures are available: Z-domain, S-domain and time domain. They allow a preliminary verification of the designing structure. Some VHDL-AMS models of SI blocks were presented in our previous paper [3].

The next step of the design process makes a conversion from the chosen prototype structure into a lower level description, suitable for a particular technique. In other words, the prototype components are replaced by an actual, transistor

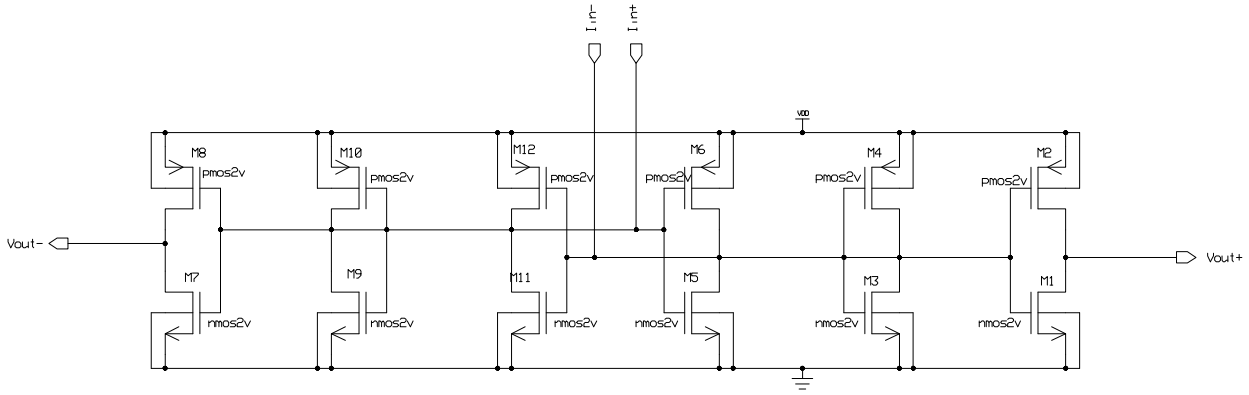

Fig. 3. Schmitt trigger used in the comparator.

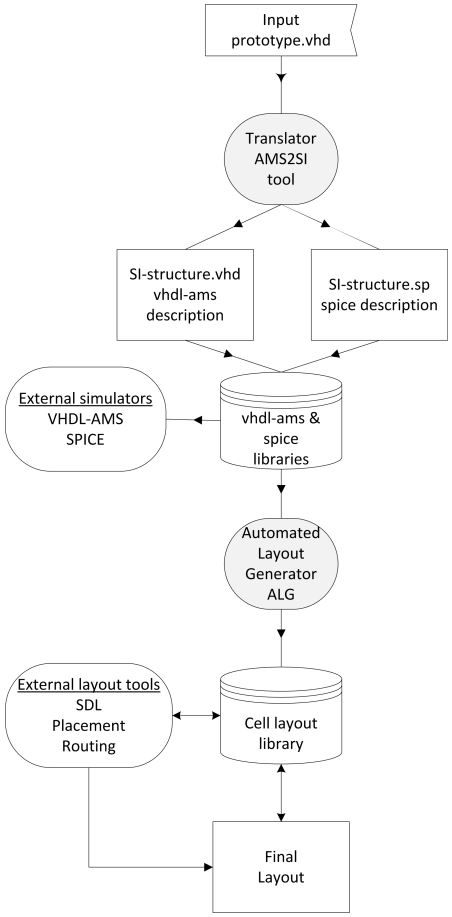

Fig. 6. Data flow in the proposed design approach.

level realization in the chosen technique. In our case it is the switched current realization. The new structure, obtained after the translation, can have different partitioning, which means some prototype entities are combined or divided into new ones. This can imply a different number of ports and interconnections. Hence, new entities must be generated, instead of just adding new architectures to the existing prototype units. Each prototype entity has its counterparts in the transistor level implementation. Taking as an example the comparator, in the prototype structure it is described as a one-input one-output block, which operates on real values. The actual realization in the SI technique is of course more complicated than presented in Fig. 2 and Fig. 3 and described above. The translation tool analyzes the input code in order to find the prototype comparator entity and replaces it with the new one, which describes the actual realization. All connections between the new versions of components are also arranged automatically by this tool. The translation rules used in this process are prepared for each prototype components. This algorithm is implemented in the AMS2SI translator tool, which is a kind of parser. The output of the conversion is again a VHDL-AMS file, but this time components used in the prototype description are replaced by new entities linked with SI blocks. Additionally, during the translation process, a file with a SPICE format description of the circuit is generated, allowing the verification at the transistor level. This automation translation is the main added value in the design flow, and provides the designer with ready-to-use implementation in a chosen technique.

B. Automated Layout Generation

After obtaining the transistor level description of the circuits, the next step of the design flow is the layout generation. The full custom designing of the layout is expensive and time-consuming task. The need to minimize costs and the time-to-market factor, forces us to find some shortcuts in this design step. One of the possible ways to improve this step is to use layout generators. For this purpose, a script language available for a particular design system can be used. Cadance system uses a SKILL language, and Mentor Graphics offers an AMPLE. In our case the AMPLE was available and it was used to code scripts to generate a layout of the system.

AMPLE is a language standard used in Mentor Graphics Common User Interface, and is common to all Falcon Framework-based applications. Using AMPLE, you can read the source code or interactively evaluate expressions, create and assign variables, define and execute new functions, and directly execute built-in functions. AMPLE supports C library and module dynamic linking to existing in house and third-party solutions bound to the Falcon Framework. AMPLE and the Common User Interface contain constructions for defining custom menus, prompt bars, forms, function keys, and strokes as well as your own functions and commands [14].

Two types of designed cells are used in our project. One is a parameterized cell and the other is a fixed cell for a given technology. Example of a parameterized one is a current mirror. The parameters of such cells can be automatically calculated using the elaborated EDA tool called Current Mirror Maker (CMM) and generated with the help of Automated Layout Generator (ALG). Both tools were integrated into one SI-Studio environment [15]. Detailed description of the tools was presented in [16]. The second type of cells, fixed cells, as integrator or comparator are taken from the created library. The information about the required interconnections of the cells are taken from the VHDL-AMS description, which was generated automatically during the translation process from the architecture level to the circuit level.

The AMPLE script was designed as an integral block of the general design flow for the automated SI circuits synthesis. The script has technology dependent parameters. It allows us to transform the prepared code to any required technology. In order to be able to use the existing tools for placement and routing, suitable restrictions for shape and size of the basic cells were assumed. The structure of the layout was designed in a way, which allows us to change the transistors' sizes and keeping the layout structure according to the cell requirements mentioned above.

IV. Example Modulator Design

As an example design a first order SDM was chosen. According to the scheme in Fig. 6 the input is a prototype structure of the SDM given in VHDL-AMS notation, which was quoted above. The prototype structure is chosen by the designer. Next the elaborated translation tool, AMS2SI, converts the prototype to the components used in the SI realization. As a result, VHDL-AMS and SPICE codes of the SDM SI implementation are obtained. The resulting VHDL-AMS code is presented below.

```
-- Generated by AMS2SI tool
-- part attached from file:  _vhdlams_begin.txt--
-- VHDL-AMS description of SIGMA-DELTA modulator
-- composed of SI blocks
--
-- File converted from Prototype SIGMA-DELTA
-- VHDL-AMS description

library ieee;
use ieee.electrical_systems.all;
use ieee.std_logic_1164.all;
use work.all;

entity Sigma_Delta_SI is
end entity Sigma_Delta_SI;

architecture SI_blocks of Sigma_Delta_SI is

terminal O_LIN_P, O_LIN_M, O_INT_P, O_INT_M
terminal OUT_SD1_P, OUT_SD1_M : electrical;
terminal O_DAC1_P, O_DAC1_M, O_DAC2_P, O_DAC2_M : electrical;
terminal CLKP, CLKM : electrical;

begin
INT1 : entity WORK.SI_INT
port map(INP=>IN_SD1_P, INM=>IN_SD1_M,
OUTP=>O_INT_P, OUTM=>O_INT_M, CLKP=>CLKP, CLKM=>CLKM);

COMP1 : entity WORK.SI_COMPARATOR
port map(INP=>O_INT_P, INM=>O_INT_M,
OUT_P=>OUT_SD1_P, OUT_M=>OUT_SD1_M);

DAC1 : entity WORK.SI_DAC1B
port map(INP=>OUT_SD1_P, INM=>OUT_SD1_M,
OUT1P=>IN_SD1_P, OUT1M=>IN_SD1_M,OUT2P=>IN_SD12_P,
OUT2M=>IN_SD12_M, CLKP=>CLKP, CLKM=>CLKM);

---part attached from file:  _vhdlams_end.txt--
end architecture SI_blocks;
```

TABLE I
SI Sigma Delta Modulator Summary of Performance

Technology	TSMC 0.18 μm CMOS
Supply Voltage	1.8 V
Resolution	6 bits
Power Consumption	1.72 μW
Bandwidth	50 kHz
Sampling Frequency	12.5 MHz
OSR	254
DNL	0.8 LSB
INL	0.9 LSB
SNR	39 dB
ENOB	6 bits
FOM	268.75 pJ

The generated structure of the SDM can be used in further steps of the design, i.e. in the layout generation. In our case the layout was generated using the ALG tool, combining with generally available tools to draw the layout as a schematic driving layout, automatic placement and routing. The final layout is presented in Fig. 7.

The performance of the resulting circuit was verified based on postlayout simulations. The Mentor Graphics Calibre tool was applied to extract the netlist with parasitics. In order to find the optimal oversampling ratio (OSR) Differential Nonlinearity (DNL) and Integral Nonlinearity (INL) errors were calculated. The calculations yielded OSR=254 as an optimal OSR value. With these parameters a 6-bit resolution was achieved. The summary performance parameters of the designed modulator are presented in Tab. I.

V. Conclusion

The paper presents the approach to the Sigma-Delta modulator design based on the VHDL-AMS description. This language was chosen to describe the initial, prototype sigma-delta modulator structure. This general structural description can be used in preliminary behavioral verification. Next, with the help of elaborated AMS2SI tool, the prototype structure is translated into an SI implementation. The generated circuit is coded in VHDL-AMS and SPICE formats. These files are used in further design steps, i.e. in the layout generation. This stage is supported by Automated Layout Generator (ALG) tool together with the regular tools used in layout design. The whole conception has been verified based on first order SI sigma-delta modulator. The layout of the circuit in TSMC $0.18\mu m$ technology was designed and postlayout simulation results are presented.

References

[1] J.M. de la Rosa. Sigma-delta modulators: Tutorial overview, design guide, and state-of-the-art survey. *Circuits and Systems I: Regular Papers, IEEE Transactions on*, 58(1):1–21, Jan. 2011.

[2] M. Voelker, J. Hauer, and J. Sauerer. Prospect of the future of switched-current circtuits with regard to future cmos technologies. *Microelectronics Journal*, 39:286–292, 2008.

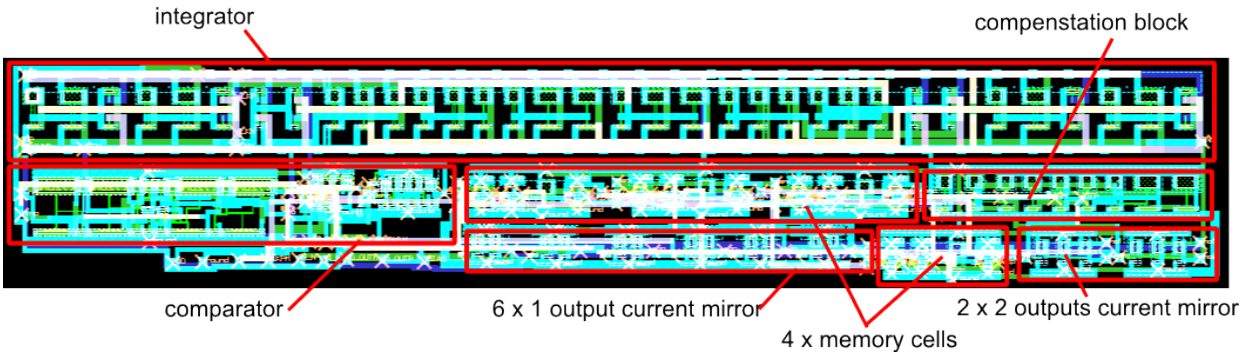

Fig. 7. Sigma-delta modulator layout.

[3] P. Śniatała, J. Pierzchlewski, and A. Handkiewicz. VHDL-AMS models for SI systems design. In *Proceedings of the 15th Mixed Design of Integrated Circuits and Systems, MIXDES'2008, ISBN 83-922632-7-8.*, pages 455–459, 2008.

[4] A. Handkiewicz, P. Śniatała, M. Łukowiak, and M. Kropidłowski. Properties of bilinear SI integrators composed of a complementary memory cell. *Journal of Electron Technology*, 32–3:247–250, 1999.

[5] A. Handkiewicz. *Mixed-Signal Systems - A Guide to CMOS Circuit Design*. Wiley-Interscience, 2002.

[6] J.B. Hughes, C. Neil, N.C. Bird, and I.C. Macbeth. Switched-currents – a new technique for analog sampled-data signal processing. In *Proceedings of the IEEE International Symposium on Circuits and Systems*, pages 1584–1587, May 1989.

[7] J. B. Hughes, Ian C. Macbeth, and Douglas M. Pattullo. Second generation switched-current signal processing. In *Proceedings - IEEE International Symposium on Circuits and Systems*, volume 4, pages 2805–2808, 1990.

[8] A. Handkiewicz, Rudnicki R., and Kropidłowski M. Switched current filter design with the use of integrators composed of equal size transistors. In *Proceedings of European Conference on Circuit Theory and Design, ECCTD'2005, Ireland,ISBN: 0-7803-9067-9*, 2005.

[9] Sz. Szczęsny. Computer tools for layout generation of switched-current circuits. PhD thesis, Technical University of Poznań, 2013.

[10] Nianxiong Tan. *Switched-Current Design and Implementation of Oversampling A/D Converters*. Kluwer Academic Publishers, Dordrecht, 1997.

[11] H. Traff. Novel approach to high speed CMOS current comparators. *Electronics Letters*, 28:310–312, 1992.

[12] D. Banks and C. Toumazou. Low-power high-speed current comparator design. *Electronics Letters*, 44 no.3,:171–172, 2008.

[13] Hae-Seung Lee, Lane Brooks, and Charles G. Sodini. Zero-crossing-based ultra-low-power a/d converters. *Proceedings of the IEEE*, 98(2):315–332, 2010.

[14] Mentor Graphics. *AMPLE for IC Flow User's Manual.*, 2003.

[15] Sz. Szczęsny, M. Naumowicz, and A. Handkiewicz. SI-studio – environment for SI circuits design automation. *Bulletin of the Polish Academy of Sciences, Technical Sciences*, 2012:757–762.

[16] P. Śniatała and R. Rudnicki. Automated design and layout generation for switched current circuits. In *Proceedings of IEEE International Symposium on Circuits and Systems (ISCAS 2006), ISBN: 0-7803-9390-2.*, pages 637–640, 2006.