

# Design of an Ultra-Low Power CT $\Sigma\Delta$ A/D Modulator in 65 nm CMOS for Cardiac Pacemakers: From System Synthesis to Circuit Implementation

Yelin Wang and Hao Cai

**Abstract**—A high performance, ultra-low power, fully differential  $2^{nd}$ -order continuous-time  $\Sigma\Delta$  analogue-to-digital modulator for cardiac pacemakers is presented in this paper. The entire design procedure is described in detail from the high-level system synthesis in both discrete and continuous-time domain, to the low-level circuit implementation of key functional blocks of the modulator. The power consumption of the designed modulator is rated at 182 nA from a 1.2 V power supply, meeting the ultra-low power requirement of the cardiac pacemaker applications. A 65 nm CMOS technology is employed to implement the  $\Sigma\Delta$  modulator. The modulator achieves a simulated SNR of 53.8 dB over a 400 Hz signal bandwidth, with 32 KHz sampling frequency and an oversampling ratio of 40. The active area of the modulator is  $0.45 \times 0.50 \text{ mm}^2$ .

**Keywords**—cardiac pacemaker, CMOS, ultra-low power, analogue-to-digital, Sigma-Delta modulation, continuous-time

## I. INTRODUCTION

As the industry of the medical implantable devices develops, lowering power consumption as much as possible is essential in improving the service time of battery, which cannot be replaced frequently. Implantable cardiac pacemaker using transistors were introduced in the 1950s, which is used to treat bradyarrhythmia [1]. The pacemaker detects the natural heart beat of the patient. If the detected heart beat gets lower than the default pace, the pacemaker then produces electrical stimulus and recovers the default pace. The service time of a common pacemaker is about five to ten years nowadays [2]. To make a pacemaker stay active as long as possible, low-power high-performance designs of the internal ICs are highly required.

A sensing unit is essential in a cardiac pacemaker. It monitors the natural activities of the heart and converts the detected electrical (analog) signals to digital quantities, which are then further processed by a digital-signal-processing (DSP) unit followed. Converting the analog signals to digital quantities helps precise signal processing and is accomplished with a low-power analog-to-digital converter (ADC). The continuous-time (CT) Sigma-Delta ( $\Sigma\Delta$ ) modulator is a good candidate for low-power ADCs design [3]–[8]. Figure 1 shows a basic CT  $\Sigma\Delta$  modulator. In CT  $\Sigma\Delta$  modulation, the spectrum of the noise is shaped by noise shaping capability achieved through the feedback path. As a result, the in-band noise is significantly decreased as most of it is shifted towards high frequencies. In

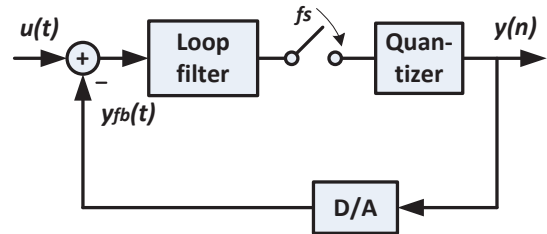


Fig. 1. Block diagram of continuous-time delta-sigma modulator system.

this way, a relatively high in-band signal-to-noise ratio (SNR) can be achieved. Another advantage of the CT  $\Sigma\Delta$  modulation lies in the fact that CT structure possesses good quality of inherent anti-aliasing, which simplifies the system design by eliminating the need for the anti-aliasing filter. In turn, power consumption introduced by the anti-aliasing filter is avoided [4]. In addition, for CT structure sampling of the analogue signal happens at the output of the loop filter so that the error introduced by imperfections of the sampling process can be largely suppressed by noise shaping.

In this work, a fully differential  $2^{nd}$ -order CT  $\Sigma\Delta$  modulator is designed. From simulation, 53.8 dB SNR is achieved over 400 Hz bandwidth under a low oversampling ratio (OSR) of 40. The power consumption is only 182 nA with 1.2 V supply voltage. The modulator is designed using the classic Boser-Wooley structure, which is rather simple and straightforward, and belongs to the Cascade of Integrators with Distributed Feedback and Coupling (CIFB) architecture [3], [9]. Active RC integrators are employed to make the  $2^{nd}$ -order loop filter because of their simplicity and good linearity. Return-to-Zero (RZ) feedback waveform is realized by a switch-based digital-to-analogue converter (DAC) in order to reduce the effect of excess loop delay. A discrete-time (DT)  $\Sigma\Delta$  modulator is first synthesized in MATLAB and then converted to the CT equivalent using Verilog-A models. Optimal design parameters are obtained through simulations on the Verilog-A CT system. Finally, the CT  $\Sigma\Delta$  modulator is implemented using a 65 nm CMOS process in Cadence design tools. The paper is organized as follows. Section II describes the high-level design including system synthesis and DT to CT modulator conversion and other issues. In Section III, low-level circuit design of each block in the CT  $\Sigma\Delta$  modulator is illustrated and discussed. Post-layout simulation result is shown in Section IV, followed by conclusions in Section V.

Y. Wang is with the Department of Electronic Systems, Aalborg University, Niels Jernes Vej 12, 9220 Aalborg East, Denmark (e-mail: walyer\_wong@hotmail.com).

H. Cai is with Institut Telecom, Telecom ParisTech, 46 Rue Barrault, 75013 Paris, France (e-mail: cai@enst.fr).

## II. HIGH-LEVEL SYSTEM SYNTHESIS

The basic concepts and methodologies for system synthesis of DT and CT  $\Sigma\Delta$  modulators are elaborated in this section. Optimal design parameters, such as gain and bandwidth of the integrator operational amplifiers, are acquired by system simulations, providing essential guidance for circuit implementation.

### A. DT $\Sigma\Delta$ Modulator Synthesis

A  $\Sigma\Delta$  A/D modulator shown in Fig. 1 can be modelled by a composition of signal transfer function (STF) and noise transfer function (NTF). Assume that the transfer function of the loop filter is represented as  $G(z)$ , the STF and NTF can be written as:

$$STF(z) = \frac{G(z)}{1 + G(z)} \quad (1)$$

$$NTF(z) = \frac{1}{1 + G(z)} \quad (2)$$

and the modulator can be represented by:

$$Y(z) = STF(z)U(z) + NTF(z)E(z) \quad (3)$$

where  $Y(z)$ ,  $U(z)$  and  $E(z)$  are the modulator output, input and the quantisation noise, respectively.

As the first step in the design of a  $\Sigma\Delta$  modulator, the NTF needs to be determined. Since the Boser-Wooley structure is used in the design, the NTF of the system in DT domain is described as [9]:

$$NTF = (1 - z^{-1})^2 \quad (4)$$

The NTF can be easily synthesized using the Delta-Sigma Toolbox, and the feed-forward and feedback coefficients are determined by the toolbox as well [3]. Figure 2a shows the synthesised DT  $\Sigma\Delta$  modulator. The loop filter is composed of two cascaded integrators, followed by a single bit quantizer. The feedback DAC generates the required feedback waveform. The purpose of synthesizing the DT  $\Sigma\Delta$  modulator is to figure out values of the coefficients in the system. With these coefficients the conversion from DT to CT system can be

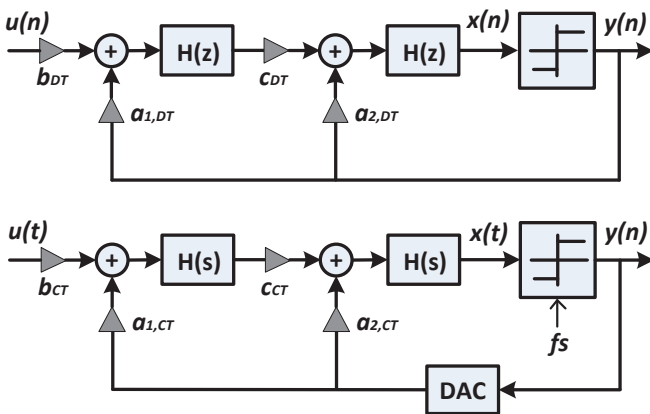


Fig. 2. (a) Block diagram of the synthesised  $2^{nd}$ -order DT  $\Sigma\Delta$  modulator,  $H(z) = \frac{z^{-1}}{1-z^{-1}}$ ; (b) the CT equivalent,  $H(s) = \frac{f_s}{s}$ .

performed. The coefficients are illustrated in Fig. 2a and their values are as follows:  $a_{1,DT} = -1$ ,  $a_{2,DT} = -2$ ,  $b_{DT} = 1$ ,  $c_{DT} = 1$ . Figure 3 plots the simulated SQNR as a function of the amplitude of input sinusoidal signal in  $dB_{FS}$ . The frequency of the input signal is at 401 Hz, and the OSR is equal to 40 (sampling frequency is 32 kHz). From the curve it can be observed that the peak SQNR of 61.6 dB is obtained when the amplitude of the input signal is around  $-6 dB_{FS}$ .

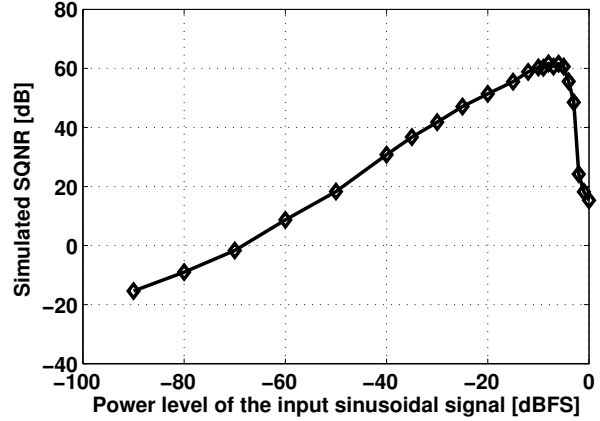


Fig. 3. Simulated SQNR versus the amplitude of the input sinusoidal signal of the synthesised DT  $\Sigma\Delta$  modulator system.

### B. Return-to-Zero Feedback Waveform

Before converting the DT system to its CT equivalent, the shape of the feedback waveform (the output of the feedback DAC) needs to be determined first, since the scheme of the conversion depends on it. Two types of feedback waveforms are commonly used in  $\Sigma\Delta$  modulation: non-return-to-zero (NRZ) and return-to-zero (RZ), as described in Fig. 4. The main difference between the two types lies in whether the same status (i.e., digital “0” or “1”) lasts an entire clock period or not. Take the first clock period in Fig. 4 for an example. In NRZ type, status “1” holds on for the whole clock period  $[0, T_S]$ ; but in RZ type, status “1” holds on only for part of the clock period  $[0, \alpha \cdot T_S]$ , where  $\alpha, \beta \in (0, 1)$ , and returns to the “reset” or “common-mode” status in the period  $[\alpha \cdot T_S, T_S]$  and  $[\beta \cdot T_S, T_S]$ .

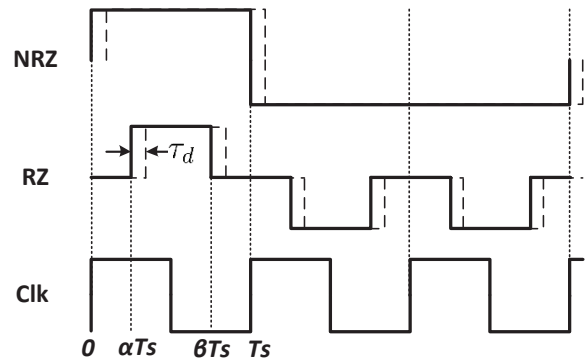


Fig. 4. NRZ and RZ feedback waveforms used in  $\Sigma\Delta$  modulator system.

One main concern when choosing the type of feedback waveform is the effect of excess loop delay, which arises from the propagation time and status settling time in quantizer, latches, flip-flops and DAC included in the system. As illustrated by the dashed waveforms in Fig. 4, with an excess loop delay time of  $\tau_d$ , the desired waveforms are shifted by the delay to be within  $[\tau_d, T_S + \tau_d]$  for NRZ case and  $[\alpha \cdot T_S + \tau_d, \beta \cdot T_S + \tau_d]$  for RZ case. The start and stop time instants of the feedback waveform are key parameters to figure out the new system coefficients during the DT-to-CT conversion. Shift in the time instants means mismatch occurs between the system coefficients and the real behaviour, which causes degradation in the dynamic performance. Figure 5 shows the simulation results of SNR versus excess loop delay  $\tau_d$  for both NRZ and RZ  $\Sigma\Delta$  modulators (for RZ case,  $\alpha = 0.25$ ,  $\beta = 0.75$ ). It can be observed that the RZ system has much better tolerance to excess loop delay than the NRZ system in terms of dynamic performance: For RZ system less than 1 dB degradation on SNR is observed when  $\tau_d$  equals to  $0.25 \cdot T_S$ ; while for NRZ case the dynamic performance is deteriorated by more than 8 dB at the same  $\tau_d$ . For the system to be more robust against excess loop delay, RZ feedback scheme is chosen in this work.

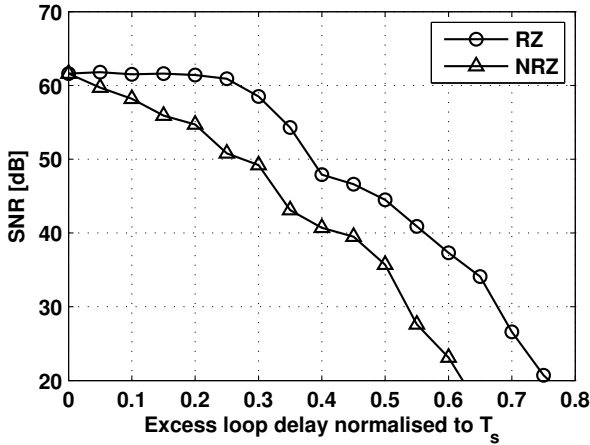


Fig. 5. Effect of excess loop delay on the dynamic performance of the  $\Sigma\Delta$  modulator system.

### C. DT-to-CT System Conversion

Among many methods to perform DT-to-CT system conversion, the *impulse-invariant transformation* is chosen [4]. To ensure the DT  $\Sigma\Delta$  modulator and its CT counterpart functioning in the same way, at every sampling instant the input signals to the quantizers in DT and CT systems should be equal to each other. This can be represented by:

$$x(n) = x(t)|_{t=n \cdot T_S} \quad (5)$$

where  $x(n)$  and  $x(t)$  represent the inputs to the quantizers in the DT and CT  $\Sigma\Delta$  modulators, respectively (as seen in Fig. 2). To make this condition always fulfilled, the transfer

functions (TF) from the modulator output  $y(n)$  to the quantizer input ( $x(n)$  and  $x(t)$ ) must be the same for DT and CT systems, which is illustrated by:

$$TF(z) = a_{1,DT} \cdot H^2(z) + a_{2,DT} \cdot H(z) \quad (6a)$$

$$TF(s) = a_{1,CT} \cdot H^2(s) + a_{2,CT} \cdot H(s) \quad (6b)$$

$$TF(z)|_{Z \rightarrow S} \equiv TF(s) \quad (6c)$$

By following the Z-to-S domain transformation and mathematical deduction described in [4], the relationship between the system coefficients of DT and CT  $\Sigma\Delta$  modulators can be obtained:

$$a_{1,CT} = \frac{1}{\beta - \alpha} \cdot a_{1,DT} \quad (7)$$

$$a_{2,CT} = \frac{1}{2} \cdot \frac{\alpha + \beta - 2}{\beta - \alpha} \cdot a_{1,DT} + \frac{1}{\beta - \alpha} \cdot a_{2,DT} \quad (8)$$

$$b_{CT} = b_{DT} \quad (9)$$

$$c_{CT} = c_{DT} \quad (10)$$

where  $\alpha = 0.25$  and  $\beta = 0.75$  represent the start and stop time instants of the RZ feedback waveform as described previously. From the DT system synthesis, values of the coefficients are obtained:  $a_{1,DT} = -1$ ,  $a_{2,DT} = -2$ ,  $b_{DT} = 1$ ,  $c_{DT} = 1$ , which results in the values of the coefficients in the CT equivalent:  $a_{1,CT} = -2$ ,  $a_{2,CT} = -3$ ,  $b_{CT} = 1$ ,  $c_{CT} = 1$ . However, these coefficients cannot be directly used in the design since they are unscaled. Coefficient scaling is essential to properly limit the inner states of the modulator, i.e., outputs of the two integrators, which ensures that the integrators remain in their linear region all the time and the quantizer is never overloaded as well. For this work, the scaling factors are chosen as  $k_1 = 8$  and  $k_2 = 16$ , resulting the scaled system coefficients for CT  $\Sigma\Delta$  modulator,  $a_{1,CT,S} = -0.25$ ,  $a_{2,CT,S} = -0.1875$ ,  $b_{CT,S} = 0.125$ ,  $c_{CT,S} = 0.5$ , where the concept and calculation are illustrated in Fig. 6. Take the first integrator (more close to the input) of the system as an example.  $a_{1,CT}$  and  $b_{CT}$  are a pair of corresponding coefficients to the first integrator. To scale them down, both are divided by the scaling factor  $k_1$  ( $= 8$ ), resulting  $a_{1,CT,S}$  and  $b_{CT,S}$ . At the output of the first integrator, the output coefficient  $c_{CT}$  (which is also the feedforward input coefficient to the second integrator) is multiplied by  $k_1$  to compensate the decrease in the output due to the scaling at the input. The same concept is applied to scale the coefficients for the second integrator.

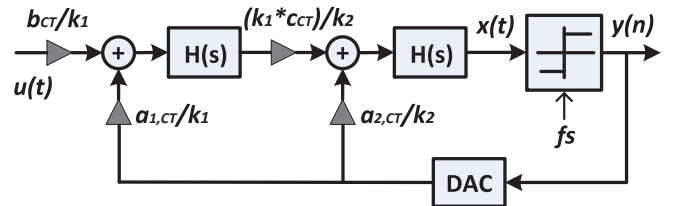


Fig. 6. Block diagram of the synthesized  $2^{nd}$ -order CT  $\Sigma\Delta$  modulator with scaled system coefficients.

#### D. CT $\Sigma\Delta$ Modulator Synthesis and Simulation

Figure 7 illustrates the schematic of the synthesized CT modulator. The loop filter contains two cascaded active RC-integrators. Values of the passive components can be figured out from the system coefficients obtained previously. The integrator op-amps are modelled as a function of the unity-gain bandwidth ( $GBW$ ) and DC gain ( $A_{DC}$ ), represented as a composition of a RC network and a voltage-controlled-voltage-source (VCVS). The comparator and DAC are modelled as ideal functional blocks using Verilog-A.

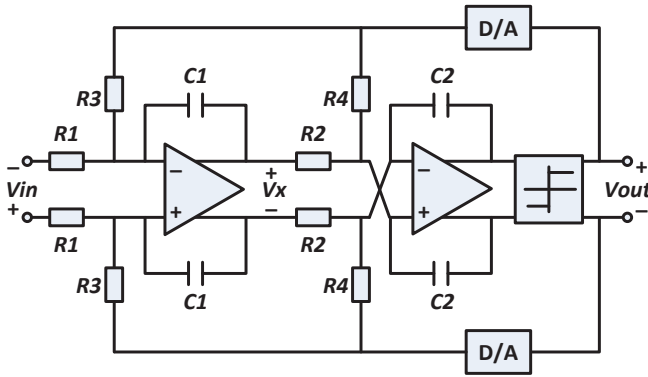


Fig. 7. Schematic of the synthesized CT  $\Sigma\Delta$  modulator.

System simulations are performed to determine the values of  $A_{DC}$  and  $GBW$  which will be used as the design targets when implementing the op-amps in hardware afterwards. To determine  $A_{DC}$ ,  $GBW$  is set closed to 'infinity' to isolate its effect on the dynamic performance of the system. Table I lists the simulated SNR of the synthesized CT system under different  $A_{DC}$  of the op-amps. It can be observed that the SNR does not degrade obviously until  $A_{DC}$  decreases under, i.e., 40 in our case. Figure 8 shows more simulation results on the issue. SNR versus OSR with different  $A_{DC}$  are plotted. It can be observed that for low to medium OSR (i.e.,  $OSR \leq 50$ ) the dynamic performance will not degrade significantly as long as  $A_{DC}$  is in the same order as/comparable to the OSR of the system. From this perspective, it is chosen that  $A_{DC}$  is targeted

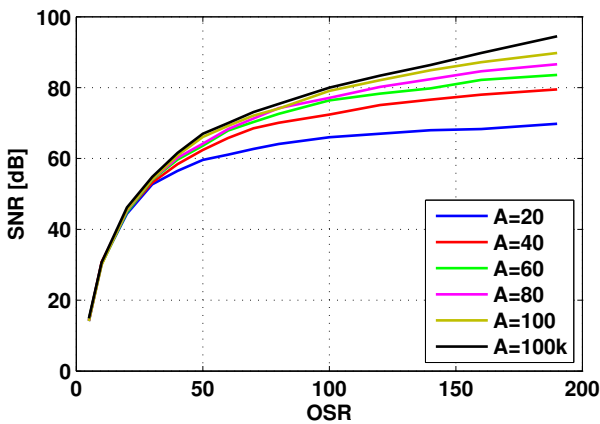


Fig. 8. Simulated SNR versus OSR with different  $A_{DC}$  of the CT  $\Sigma\Delta$  modulator.

TABLE I  
SNR OF THE SYSTEM WITH DIFFERENT OP-AMP  $A_{DC}$

$A_{DC}$ (linear scale)	SNR (dB)
20	56.5
40	59.3
60	60.1
80	60.6
100	61.0

TABLE II  
SNR OF THE SYSTEM WITH DIFFERENT OP-AMP  $GBW$

$GBW$ (Hz)	SNR (dB)
$2 \times f_s$	55.3
$3 \times f_s$	58.2
$4 \times f_s$	59.1
$5 \times f_s$	60.3

in the range of 40-60 for later circuit design, considering the trade-off between the power consumption and the performance of the op-amp.

Similar simulations are performed in order to determine the target  $GBW$  of the op-amp. Table II lists the simulated SNR under different  $GBW$  values, which are represented as multiples of the sampling frequency  $f_s$  ( $f_s = 32 \text{ kHz}$ ). It can be seen that the dynamic performance of the system has little improvement with  $GBW$  increasing from 3 to 5 times of  $f_s$  (and higher multiples). Considering the requirement of low power consumption,  $GBW$  between 3 to 4 times of  $f_s$  is determined as the design target in later circuit implementation.

Finally, system simulation is performed with the selected values of  $A_{DC}$  and  $GBW$ , which provides an initial figure of how much SNR can be obtained. Figure 9 plots the simulated output spectrum of the synthesised CT  $\Sigma\Delta$  modulator with op-amp  $A_{DC}$  and  $GBW$  of 40 and  $3 \times f_s$  (96 kHz), respectively. A SNR of 56.2 dB is achieved under a sinusoidal input signal with 401 Hz frequency and  $-6 \text{ dB}_{FS}$  power level. Figure 9 plots also the simulated output spectrum of an ideal system, where the op-amp  $A_{DC}$  and  $GBW$  are set to be 'infinity'. Degradation in the dynamic performance can be observed and the SNR is deteriorated with approximately 5.4 dB.

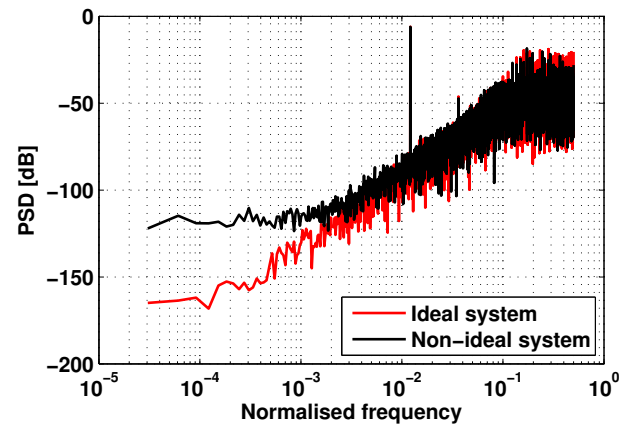


Fig. 9. Simulated output spectrum of the CT  $\Sigma\Delta$  modulator system with non-ideal and ideal op-amps in the loop filter.



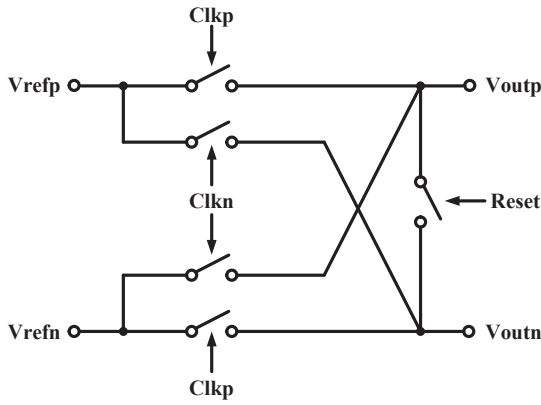


Fig. 12. Simplified symbol view of the designed DAC.

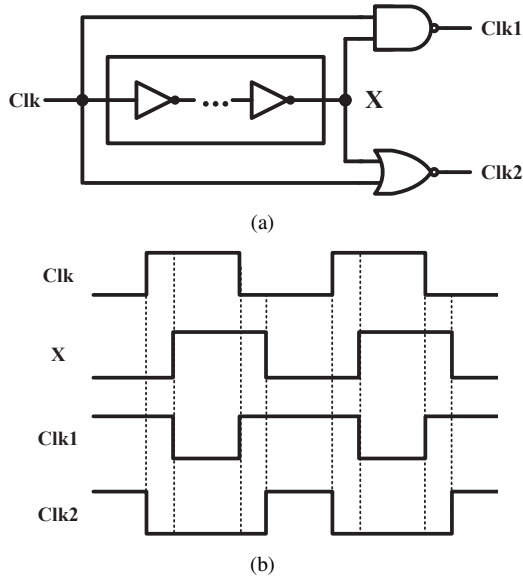


Fig. 13. Non-overlapping clocking scheme used in the DAC, (a) Symbol view of the logic employed; (b) An example of the generated non-overlapping signals,  $Clk1$  and  $Clk2$ .

is employed. Figure 13 illustrates the scheme used in the work to generate the non-overlapping clock signals and an example of the generated signals.

#### IV. POST LAYOUT SIMULATION RESULTS

Figure 14 shows the layout of the designed CT  $\Sigma\Delta$  A/D modulator with the clock generator included. It occupies an active area of  $0.45 \times 0.50 \text{ mm}^2$ , of which the majority area is used by resistance and capacitance in the modulator due to the low clock frequency (32 kHz) of the system. Common-centroid layout technique is used for transistors and passive elements as well to achieve good matching between critical elements. Post-layout simulation is performed and an SNR of 53.8 dB to the maximum has been achieved. There is slight degradation on the dynamic performance compared to the synthesised CT system, where a maximum SNR of 56.2 dB is achieved. This degradation is mainly due to the non-linearity of the large resistance used (in the magnitude of tens of  $M\Omega$ ) in the layout. Figure 15 plots the simulated SNR as

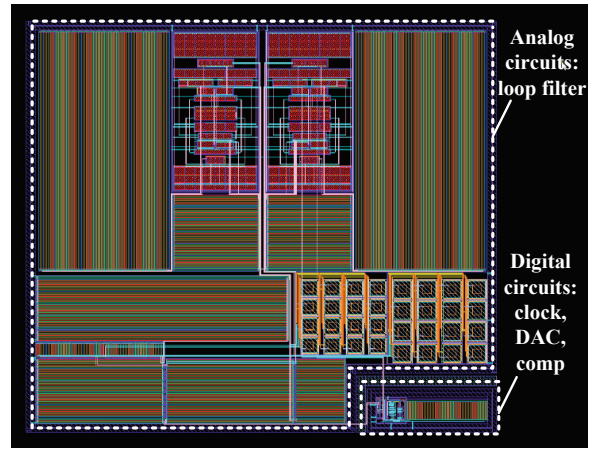


Fig. 14. Layout of the designed CT  $\Sigma\Delta$  A/D modulator.

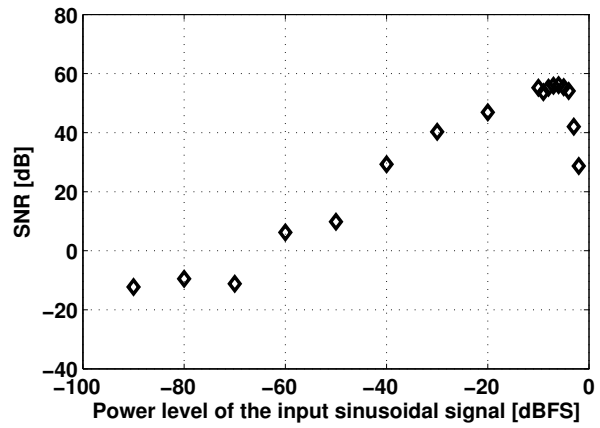


Fig. 15. Post-layout simulated SNR versus the power level of the input sinusoidal signal.

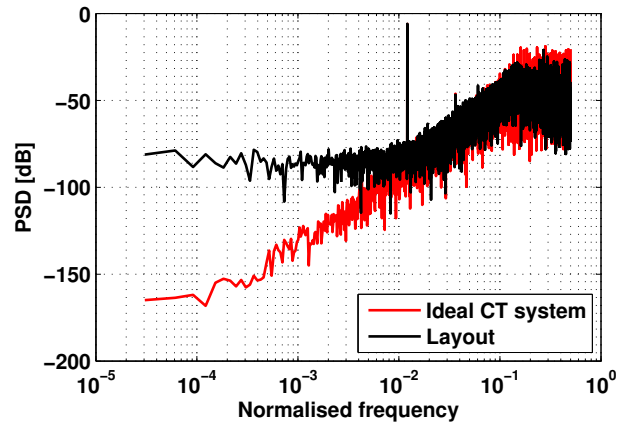


Fig. 16. Post-layout simulated output spectrum of the designed CT  $\Sigma\Delta$  A/D modulator.

a function of the power level of the input sinusoidal signal with a frequency of 401 Hz. The maximum SNR is observed around  $-6 \text{ dB}_{FS}$  power level of the input signal. The simulated output spectrum that gives the best SNR is plotted in Fig. 16. The corresponding simulated output spectrum of the ideal CT  $\Sigma\Delta$  A/D modulator (synthesised previously) is also plotted in

TABLE III  
PERFORMANCE COMPARISON OF LOW POWER ADCs DESIGN

Refs.	Architecture	Process	BW [Hz]	Sampling rate [Hz]	$V_{DD}$ [V]	ENOB [bits]	Power [nW]	FOM [pJ/conv.]	Area [ $mm^2$ ]
[12]	SAR	0.14 $\mu m$	-	3.125 k	1.2	12	850	0.066	0.35
[13]	SAR	0.18 $\mu m$	20 k	80 k	1.0	8.0	400	0.0195	0.12
[14]	SAR	0.13 $\mu m$	-	1 k	1.0	9.1	53	0.0945	0.19
[15]	SAR	0.18 $\mu m$	-	17.8 k	1.2	5.2	162.5	2.2	-
[7]	CT $\Sigma\Delta$	0.35 $\mu m$	25 k	3.2 M	3.0	9.04	4350	0.267	0.0138
[16]	SAR	0.18 $\mu m$	5 k	10k	1.1	7.4	127	0.0634	0.06
[17]	LC	0.18 $\mu m$	5-3.3 k	-	0.8	$\leq 7.9$	313-582	0.219-0.565	0.045
[18]	SAR	65 nm	-	25 k	1.0	8.0	281	0.0433	0.0174
<b>This work</b>	<b>CT <math>\Sigma\Delta</math></b>	<b>65 nm</b>	<b>400</b>	<b>32k</b>	<b>1.2</b>	<b>8.6</b>	<b>218.4</b>	<b>0.70</b>	<b>0.225</b>

Fig. 16 for comparison. The effective number of bits ( $ENOB$ ) of the system is about 8.6 bits, which is calculated by:

$$ENOB = \frac{SNR - 1.76}{6.02} \quad (11)$$

The designed CT  $\Sigma\Delta$  A/D modulator consumes about 182 nA current at 1.2 V supply voltage. Most of the power is consumed by the loop filter as indicated in previous section. The figure-of-merit (FOM) of the modulator is about 0.70 pJ/conversion step, calculated by:

$$FOM = \frac{P_{consumed}}{2 \times BW_{IN} \times 2^{ENOB}} \quad (12)$$

where  $P_{consumed}$  is the power consumption of the designed CT  $\Sigma\Delta$  A/D modulator and  $BW_{IN}$  is the bandwidth of input signal. Table III compares the performance of the design in our work and other low-power ADC designs in recent literature.

## V. CONCLUSION

This paper presents the design of a low power fully differential  $2^{nd}$ -order CT  $\Sigma\Delta$  A/D modulator in a 65 nm CMOS process. The design achieves an ultra-low power consumption of 218.4 nW, making it suitable for pacemaker applications. It may also be used for other medical implantable devices, where low power consumption is a basic design concern. Loop filter of the designed modulator are realised by two cascaded active-RC integrators. The integrator op-amps are designed using folded-cascode topology. To meet the low power consumption requirement, the transistors are constrained to be operating in the weak-inversion region. The paper elaborates the complete top-down design procedure from system synthesis to circuit implementation. Important design issues are discussed for each stage in the design. It may be used as a quick design guidance for engineers and researchers in this area.

## ACKNOWLEDGMENT

The authors thank Dejan Radjen and Martin Anderson, Lund University, Sweden, for their help and fruitful discussions throughout the whole work.

## REFERENCES

- [1] O. Aquilina, "A Brief History of Cardiac Pacing," *Images Paediatr Cardiol*, vol. 8, no. 2, pp. 17–81, 2006.
- [2] M. A. Karami and D. J. Inman, "Powering Pacemakers from Heartbeat Vibrations using Linear and Nonlinear Energy Harvesters," *Applied Physics Letters*, vol. 100, no. 4, p. 042901, 2012, doi 10.1063/1.3679102.
- [3] R. Schreier and G. C. Temes, *Understanding Delta-Sigma Data Converters*, 1st ed. Wiley-IEEE Press, November 2004, isbn 0471465852.
- [4] M. Ortmanns and F. Gerfers, *Continuous-Time Sigma-Delta A/D Conversion: Fundamentals, Performance Limits and Robust Implementations*, ser. Springer Series in Advanced Microelectronics. Springer, 2006, isbn 3540284060.
- [5] T. Song, Z. Cao, and S. Yan, "A 2.8-mW 2-MHz Continuous-Time  $\Sigma\Delta$  Modulator With a Hybrid Active-Passive Loop Filter," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 2, pp. 330–341, 2008.
- [6] J. Zhang, Y. Lian, L. Yao, and B. Shi, "A 0.6-V 82-dB 28.6-uW Continuous-Time Audio Delta-Sigma Modulator," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 10, pp. 2326–2335, 2011.
- [7] E. López-Morillo, F. Muñoz, A. Torralba, F. Márquez, I. Rebolle, and J. R. García-Oya, "Compact Low-Power Implementation for Continuous-Time  $\Sigma\Delta$  Modulators," *Integration, the VLSI Journal*, vol. 46, no. 4, pp. 441–448, 2012.
- [8] J. Garcia, S. Rodriguez, and A. Rusu, "A Low-Power CT Incremental 3rd Order  $\Sigma\Delta$  ADC for Biosensor Applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 1, pp. 25–36, 2013.
- [9] B. E. Boser and B. A. Wooley, "The Design of Sigma-Delta Modulation Analog-to-Digital Converters," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 6, pp. 1298–1308, 1988.
- [10] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*, 1st ed. Wiley, 1996, isbn 0471144487.
- [11] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, 1995.
- [12] D. De Venuto, D. T. Castro, Y. Ponomarev, and E. Stikvoort, "0.8  $\mu W$  12-bit SAR ADC Sensors Interface for RFID Applications," *Microelectronics Journal*, vol. 41, pp. 746–751, 2010.
- [13] J. H. Cheong, K. L. Chan, P. B. Khannur, K. T. Tiew, and M. Je, "A 400-nW 19.5-fJ/Conversion-Step 8-ENOB 80-kS/s SAR ADC in 0.18- $\mu m$  CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 58, no. 7, pp. 407–411, 2011.
- [14] D. Zhang, A. Bhide, and A. Alvandpour, "A 53-nW 9.1-ENOB 1-kS/s SAR ADC in 0.13- $\mu m$  CMOS for Medical Implant Devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 7, pp. 1585–1593, 2012.
- [15] I. Kianpour, M. Baghaei-Nejad, and L. Zheng, "78 nW Ultra-Low-Power 17 kS/s Two-Step-Successive Approximation Register Analogue-to-Digital Converter for RFID and Sensing Applications," *IET Circuits, Devices & Systems*, vol. 6, no. 6, pp. 397–405, 2012.
- [16] W. Hu, Y. Liu, T. Nguyen, D. Y. C. Lie, and B. P. Ginsburg, "An 8-Bit Single-Ended Ultra-Low-Power SAR ADC With a Novel DAC Switching Method and a Counter-Based Digital Control Circuitry," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 7, pp. 1726–1739, 2013.
- [17] Y. Li, D. Zhao, and W. A. Serdijn, "A Sub-Microwatt Asynchronous Level-Crossing ADC for Biomedical Applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 7, no. 2, pp. 149–157, 2013.
- [18] C. Yuan and Y. Y. H. Lam, "A 281-nW 43.3 fJ/Conversion-Step 8-ENOB 25-kS/s Asynchronous SAR ADC in 65nm CMOS for Biomedical Applications," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Beijing, China, May 2013, pp. 622–625.