Editorial

We greatly appreciate the opportunity to highlight the topic of electronic circuits testing by the International Journal of Electronics and Telecommunications.

Imperfections in the manufacturing process requires testing of hardware-implemented circuits and their components. The increasing complexity of such systems makes this issue more and more demanding. The main objective of testing is to distinguish between good and faulty ones. This objective can be achieved in several ways, e.g. by functional or structural testing. Either analog or digital, fault detection or location in electronic systems is usually performed by analysis of measurements results acquired from a limited number of inputs and outputs. This problem becomes near critical with the advent VLSI and ULSI components. For more than five decades, the subject of fault location in analog and mixed-signal circuits has been of interest to researchers. In recent ten years this interest has been intensified significantly. The device and voltage scaling scenarios for present and future nanometer CMOS technologies cause that the attention will shift to testing defects that did not exist before or that were not relevant in the past.

The scope of the following seven research papers is to consider some aspects of testing, diagnosing and tuning of analog and mixed-signal systems. We would like to note that these works include contributions that are oriented both for development of theoretical methods as well as for implementation of test procedures for real life applications. First of these papers is a comprehensive tutorial devoted to some new aspects of fault diagnosis of nonlinear analog circuits. The second one gives a parameter identification method for the specified design performances. Another one presents construction of the fuzzy logic system for analog circuits soft fault diagnosis. Some heuristic methods: GEP and differential evolution in testing of diode-transistors circuits are the topic of the next work. The other one proposes an idea of a new structure for a Test Pattern Generator enabling detection of crosstalk faults that may happen to bus-type interconnections between built-in blocks within a System on a Chip structure. The following paper presents functional test procedures for ASIC CMOS VLSI chip. Finally, automatic test bench used for measurement of selected high frequency parameters of a power copper line in context of Power Line Communication (PLC) is described and discussed.

The work as Guest Editors was facilitated by the response of authors who prepared regular contributions for this issue of IJET. We would like to thank all the authors for their splendid cooperation as well as the reviewers for their careful attention to details leading to enhance the quality of the published articles.

We are hoped that content of this issue will assist readers, particularly younger colleagues, in becoming aware of the possibilities for future contributions in this important area of electronics.

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Guest Editors